

INTERFACETM



MICROCOMPUTING FOR HOME AND SMALL BUSINESS

VOL. 2, ISSUE 3, FEB. 1977

\$1.50

Warp Factor

Microcomputer Stock Options

LEGION: Artificial Intelligence

Random Number Generator

**8080 Memory Object Code
Search Routine**

**Basic Algorithms For
Math Functions**



WHY SETTLE FOR LESS— THAN A 6800 SYSTEM

MEMORY—

All static memory with selected 2102 IC's allows processor to run at its maximum speed at all times. No refresh system is needed and no time is lost in memory refresh cycles. Each board holds 4,096 words of this proven reliable and trouble free memory. Cost—only \$125.00 for each full 4K memory.

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Serial control interface connects to any RS-232, or 20 Ma. TTY control terminal. Connectors provided for expansion of up to eight interfaces. Unique programmable interface circuits allow you to match the interface to almost any possible combination of polarity and control signal arrangements. Baud rate selection can be made on each individual interface. All this at a sensible cost of only \$35.00 for either serial, or parallel type

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"Motorola" M6800 processor with Mikbug® ROM operating system. Automatic reset and loading, plus full compatability with Motorola evaluation set software. Crystal controlled oscillator provides the clock signal for the processor and is divided down by the MC14411 to provide the various Baud rate outputs for the interface circuits. Full buffering on all data and address busses insures "glitch" free operation with full expansion of memory and interfaces.

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Heavy duty 10.0 Amp power supply capable of powering a fully expanded system of memory and interface boards. Note 25 Amp rectifier bridge and 91,000 mfd computer grade filter capacitor.

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Probably the most extensive and complete set of data available for any microprocessor system is supplied with our 6800 computer. This includes the Motorola programming manual, our own very complete assembly instructions, plus a notebook full of information that we have compiled on the system hardware and programming. This includes diagnostic programs, sample programs and even a Tic Tac Toe listing.

Mikbug® is a registered trademark of Motorola Inc.

SwTPC 6800
Computer System

with serial interface and 4,096 words
of memory. \$395.00



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Southwest Technical Products Corp., Box 32040, San Antonio, Texas 78284

Meet the most powerful μ C system available for dedicated work. Yet it's only \$595.*

*kit price

Here's the muscle you've been telling us you wanted: a powerful Cromemco microcomputer in a style and price range ideal for your dedicated computer jobs—ideal for industrial, business, instrumentation and similar applications.

It's the new Cromemco Z-2 Computer System. Here's some of what you get in the Z-2 for only \$595:

- The industry's fastest μ P board (Cromemco's highly regarded 4 MHz, 250-nanosecond cycle time board).
- The power and convenience of the well-known Z-80 μ P.
- A power supply you won't believe (+8V @ 30A, +18V and -18V @ 15A — ample power for additional peripherals such as floppy disk drives).
- A full-length shielded motherboard with 21 card slots.
- Power-on-jump circuitry to begin automatic program execution when power is turned on.
- S-100 bus.
- Standard rack-mount style construction.
- All-metal chassis and dust case.
- 110- or 220-volt operation.

DEDICATED APPLICATIONS

The new Z-2 is specifically designed as a powerful but economical dedicated computer for systems work. Notice that the front panel is entirely free of controls or switches of any kind. That makes the Z-2 virtually tamper-proof. No accidental program changes or surprise memory erasures.

FASTEST, MOST POWERFUL μ C

Cromemco's microcomputers are the fastest and most powerful available. They use the Z-80 microprocessor which is

widely regarded as the standard of the future. So you're in the technical fore with the Z-2.

BROAD SOFTWARE/PERIPHERALS SUPPORT

Since the Z-2 uses the Z-80, your present 8080 software can be used with the Z-2. Also, Cromemco offers broad software support including a monitor, assembler, and a BASIC interpreter.

The Z-2 uses the S-100 bus which is supported by the peripherals of dozens of manufacturers. Naturally, all Cromemco peripherals such as our 7-channel A/D and D/A converter, our well-known BYTESAVER with its built-in PROM programmer, our color graphics interface, etc., will also plug into the S-100 bus.

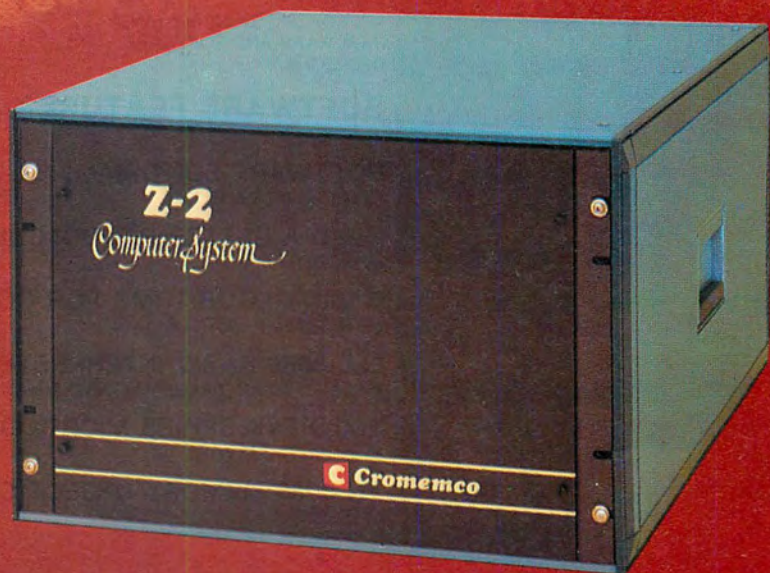
LOW, LOW PRICE

You'll be impressed with the Z-2's low price, technical excellence and quality. So see it right away at your computer store—or order directly from the factory.

Z-2 COMPUTER SYSTEM KIT (MODEL Z-2K) (includes 4 MHz μ P card, full-length 21-card-slot motherboard, power supply, one card socket and card-guide set, and front panel; for rack mounting)\$595.

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optional bench cabinet



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CIRCLE INQUIRY NO. 6



Cover Story

This month's cover is somewhat reminiscent of those first spectacular views of Mars as seen by researchers on earth as T.V. signals were beamed back over the many millions of miles through space.

In reality it is a setting for a major announcement to take place in March.

"Warp Factor" is a light hearted scenario highlighting the features of the newest microcomputer kit to enter the personal computing marketplace. Motorola is introducing the HEP EDUCATOR II, a small system designed for the economically oriented student or computer hobbyist. The total price for this nifty little box of computing tricks—\$169⁹⁵.

You may start looking for Educator II in your local Byte Shop computer store or in many of the selected HEP distributors.

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INTERFACETM AGE

MICROCOMPUTING FOR HOME AND SMALL BUSINESS

VOL. 2 ISSUE 3

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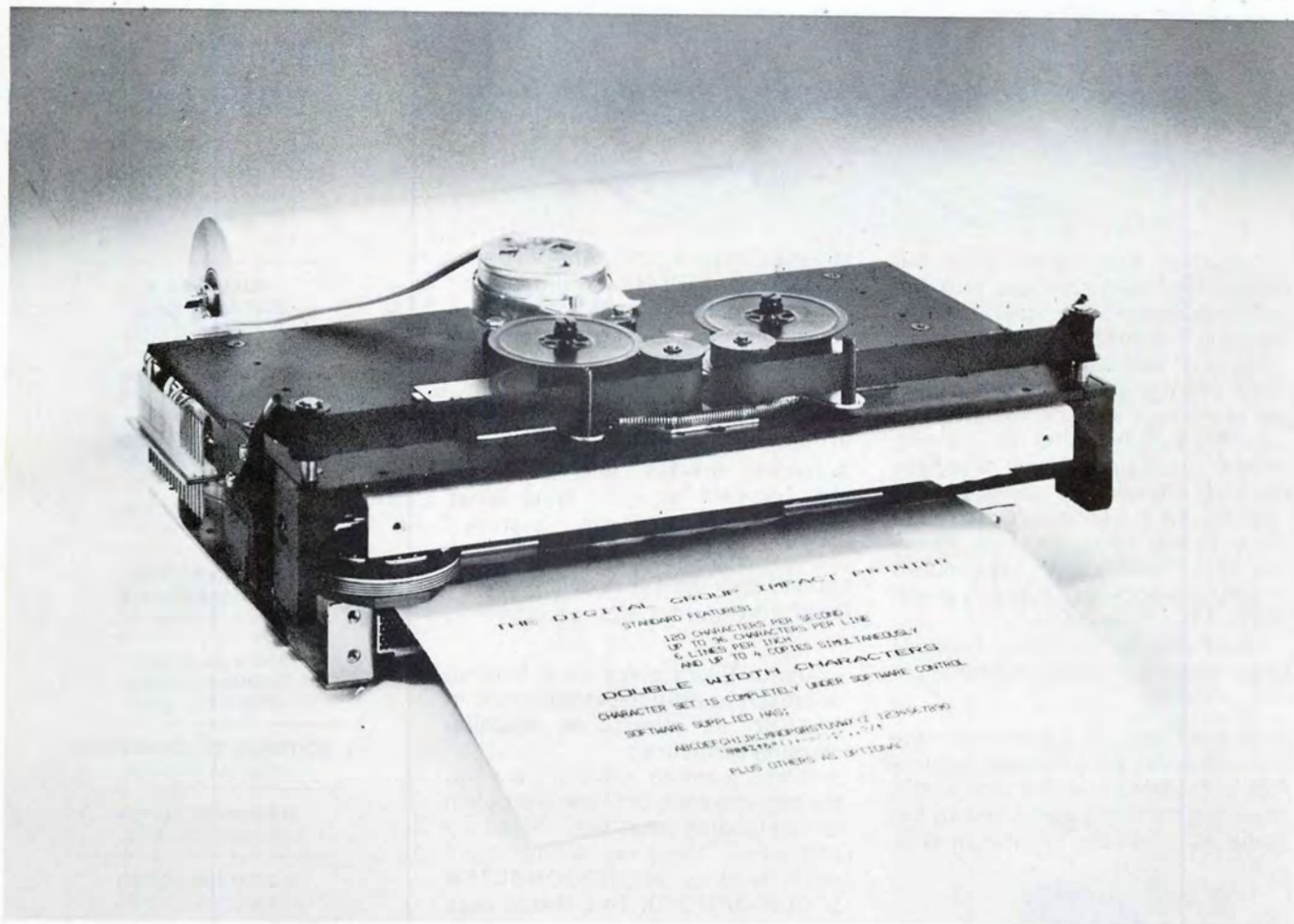
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Print Your Heart Out.

With help from the Digital Group, naturally.

Now, that small computer system you own or have been considering for personal or business use suddenly becomes a lot more usable—with the addition of a full-size *impact* printer from the Digital Group. A printer designed for small computers that need big output (like yours).

With the Digital Group printer, you can print your heart out...and it won't cost an arm and a leg. The Digital Group printer is available for less than \$500. That's right—\$500.

Just look at these specifications:

- Fast—120 characters per second
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- Makes up to 4 copies simultaneously
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- Ribbon has built-in re-inkers for a life of 10,000,000 characters
- Paper can be either a standard 8½-inch roll, fanfold or cut page
- Interfaces to 8-bit parallel ports

There are lots of capabilities and outstanding features of the Digital Group printer...and (as always) the best news is our price. Kit prices start as low as \$495 for the printer and interface card. It simply can't be beat.

Find out all the facts about the Digital Group printer now. Just fill in the coupon below or give us a call for the details. We think you'll find a place for our printer in your system...and in your heart.

the digital group

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Send me all the details on your full-size impact printer.

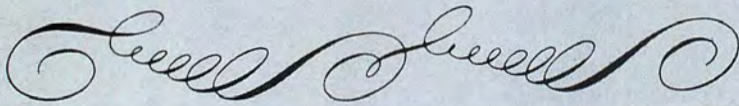
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INTERFACIAL



Departing this month from our normal immediate plunge into the goodies contained in this issue, I'm vectoring to a much requested priority.

Many of you have written asking "Who are the people whose names we see listed on the masthead?"

In this issue and for the coming several issues, we shall introduce the staff and include some of their background. It will help you to relate better to the magazine if you know who performs the tasks each month of getting a book together and eventually into your hands.

This month the Northwest Regional Editor and the Assistant Editor share the spotlight.

Dr. Adam Osborne is author of more than 50 works on computer technology and is familiar with a wide variety of assembly languages used by virtually all products on the market.



Formerly a computer systems engineer and process engineer with Shell Oil Corp., Dr. Osborne now heads his own firm, Osborne & Associates, Inc. He is a graduate of University of Birmingham, England, (B.Sc.), University of Delaware, (M.Ch.E. and Ph.D.)

Linda Folkard-Stengel has long experience in technical journalism, public relations and television journalism.



Quadrilingual, she was formerly with the Overseas Office of Design News and with the Mexico City-based official organ of the Association of

Mexican Travel Agents, AMAV News. She served as TV News Film Librarian for Canadian Broadcasting Corporation's English-language anchor station CBLT, Toronto.

This month's issue has been artfully brushed with many valuable software articles answering the ever-present moan, "Now what do I do next with my system."

To help fill your system's endless appetite Tom Doyle presents an 8080 Octal Monitor program

Marlin Ellers gives us a fanciful approach to artificial intelligence in LEGION, an attempt at machine learning techniques.

If you want to make it "big" in the stock market, but have a problem understanding what you should do and when, then, my friend, don't miss reading MICROCOMPUTER STOCK OPTIONS. This theme puts your home computer to work profitably.

Everyone has wondered when Motorola would seriously get into hobby computing. Exclusive! The beginner now has the HEP EDUCATOR II, the first step to a bubble-packed computer kit available at over 1500 electronics stores across the nation. It is coming in March, but read about it now in WARP FACTORS by Tom Mazur.

Continuing with construction projects, Roger Brown offers another approach to A/D converters for your personal computing activities. Card-of-the-Month features the TDL-ZPU™ CARD with Roger Edelson casting a qualitative eye on this popular product.

For those who have the older teletypes, not useful to home computing applications, rejoice. A possible solution to a conversion for the rigs is outlined in COMPUTER COUPLING TO TELETYPE LOOPS by B.D. Lichtenwalner.

Understanding hardware and software concepts is outlined in ultra-simplistic terms by Ken Pugh in THE BLACK BOX.

Again Bob Stevens has corraled a herd of useful software items by many talented contributors in the avocational and vocational computing fields.

INTERFACE AGE MAGAZINE

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Cerritos, CA 90701
(213) 926-6629

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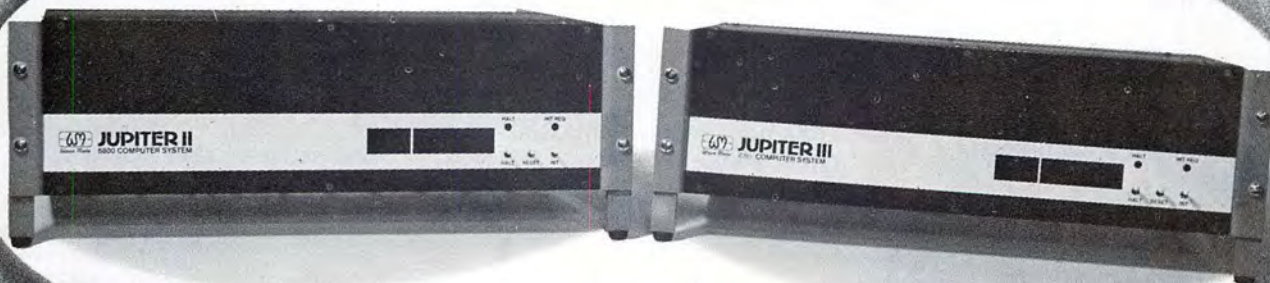
Editorial Correspondence

Direct all correspondence to the appropriate editor at: INTERFACE AGE magazine, P.O. Box 1234, Cerritos, CA 90701. Editorial contributions must be accompanied by return postage and will be handled with reasonable care, however, publisher assumes no responsibility for return or safety of manuscripts, art work, or models.

Advertising Inquiries

Direct all advertising inquiries to: Advertising Department, INTERFACE AGE magazine, 61 South Lake Avenue, P.O. Box 4566, Pasadena, CA 91106. (213) 795-7002.

POPULARITY EXPLOSION!



JUPITER II A 6800 System \$795

If you thought the quality of a wire-wrapped system was beyond your price. Take a look at what we have now!

The Jupiter IIA and the Jupiter IIIA Basic computer systems. You get the system module cage with fully assembled backplane, fully assembled plug-in ferro-resonant power supply, front panel kit and your choice of 6800 or Z80 CPU module kit. All less than the price of the two best selling 8080 systems!

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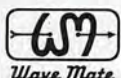
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Update

NATIONAL SEMICONDUCTOR ANNOUNCES MICROPROCESSOR COURSES

Santa Clara, CA . . . National Semiconductor Corp. is offering a series of microprocessor training courses at its Santa Clara, California, facility, as well as SC/MP application courses in various western U.S. cities.

At National Semiconductor's Western Microprocessor Training Center, 1333 Lawrence Expressway, Santa Clara, CA, courses will be given in Microprocessor Fundamentals February 21-24, March 21-24, April 18-21, and June 6-9. Courses in Advanced Programming are scheduled for February 7-10 and May 9-12.

Courses on the application of National's PACE microprocessor will be offered at the Western Training Center on February 28 - March 3, April 25-28, and June 13-16. SC/MP application courses will be given March 7-10, March 28-31, May 2-5, and June 20-23.

In addition, courses on the applications of SC/MP (Simple, Cost-Effective Microprocessor) will be presented in Seattle, Washington, on February 14-18; in Edmonton, Canada, on February 21-25; in Denver, Colorado, March 14-18; and in Orange County, California, April 4-8. Class hours are 10 a.m. to 5 p.m.

The five-day courses given in the field include either a free SC/MP kit of a free SC/MP keyboard kit in the total fee of \$395. The sessions discuss the fundamentals and tools of SC/MP microprocessors in detail to allow the student to solve any application problems he may encounter. They include complete SC/MP lab stations with one instructor for every six students for close lab supervision. In addition, the field courses feature hands-on time on two 16-bit IMP microprocessor systems (floppy disc) for high-speed software development and PROM programming.

Registration information may be obtained from local National Semiconductor sales offices or from National's Western Microprocessor

Training Center in Santa Clara, California, (408) 247-7924.

AIAA SEMINAR ON PROPOSAL PREPARATION

A seminar in proposal preparation is to be held at Gene Autry Hotel, Palm Springs, California March 3-4, 1977 and at Hyatt/Union Square, San Francisco June 2-3, 1977. Sponsored by the American Institute of Aeronautics and Astronautics (AIAA), this two-day seminar deals exclusively with the methods for winning new business via the proposal route. The main themes propose to instruct how high technology products and services are procured by various U.S. government agencies and how the customer picks the winners. Presented over seventy times in three years in public and inhouse versions, the seminar has been consistently rated from excellent to outstanding by its over 3,000 attendees from some 200 companies, 80 government agencies and 50 universities.

The seminar is in nine parts under the following headings:

Part 1: The Ideal Proposal Organization - Authority and Responsibility; Part 2: The Important Pre-proposal Programs; Part 3: Initiation of the Proposal Effort; Part 4: How, When and Where to Spend Resources; Part 5: Learning to Communicate in a Written Proposal; Part 6: the Source Selection Process; Part 7: Actual Preparation of the Various Proposal Sections; Part 8: Post-proposal Activities and Tricks of the Trade. Registration information for individuals and groups may be obtained from AIAA Seminar, 444 W. Ocean Bl. P.O. Box 1710, Suite 1403, Long Beach, CA 90801 - 213 437-7465.

NEW CLUB

A new club is being formed for the exchange of information on use of Heathkit products by computer hobbyists. Write: Computer Heathkit Users' Group, c/o Charles Floto, 267 A Willow St., New Haven, CT 06511.

TRENTON COMPUTER FESTIVAL

The Second Trenton Computer Festival will be held at Trenton State College, Route 1, Trenton, N. J. from April 30, 1977 to May 1, 1977. Featured are a special conference sponsored by IEEE on consumer and hobby applications of microcomputers, exhibits, displays, contests, a huge flea market for hardware and software and manufacturers' booths.

General registration is \$4.00 with a special students' rate of \$2.00 and sales \$2.00 per spot. For advanced registration or information call Jaci Di Paolo at (609) 771-2487 or write Trenton Computer Festival, Trenton State College, Trenton N. J. 08625.

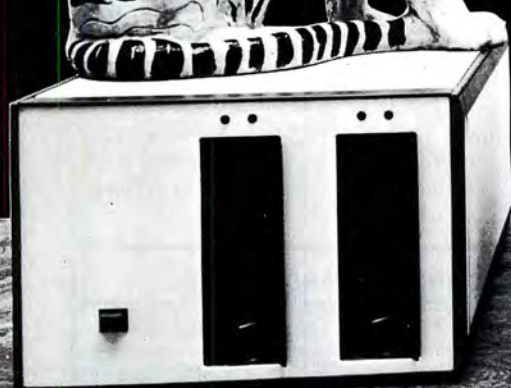
CALENDAR

- Feb. 1 El Paso Computer Group meets at 7:00 p.m. for meetings place call (915) 544-1542.
- Feb. 2 New England Computer Society, Inc. meets at 7:00 p.m. MITRE Corp., Cafeteria, Route 62 Bedford, MA. Call Dave Day at (603) 434-4239 for more information.
- Feb. 2 Northwest Computer Club meets at 7:00 p.m., Pacific Science Center. Seattle, WA. Informal meetings. Details by calling (206) 524-6359.
- Feb. 5 Louisville Area Computer Club meets at 1:00 p.m., Speed Auditorium, University of Louisville. General meetings, Contact Glen Darwin (502) 456-5589 or write 3028 Hunsinger Ln., Louisville, KY: 40200.
- Feb. 6 Orange County Computer Club meets at 12:00 noon, California State University Fullerton, Administration Bldg., Room 321. For meeting agenda call: Lorin Mohler at (714) 998-5831.
- Feb. 11 Crescent City Computer Club meets at 8:00 p.m., University of New Orleans, Lakefront Campus. For more information contact Bob Latham (504) 722-6321.
- Feb. 11 Rochester Area Micro-computer Society meets at 6:30 p.m., Room 1030, Bldg. 9, Rochester, NY. Mailing address, RAMS, P.O. Box D, Rochester NY 14609.



G R-R-R-eat

The NEW Sphere DOS - a Real Tiger!!



When we decided to redesign our already successful Disk Operating System, we asked ourselves how we would want it done. Based on a year of solid experience building, shipping and supporting a good DOS, we decided we would want our new DOS to be able to:

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Over 8000 definitions and explanations of terms and concepts relating to microprocessors, microcontrollers and microcomputers. Special sections on programmable calculators; math and statistics definitions; flow chart symbols and techniques; binary numbers and other related computer terms. There is also a comprehensive electronic/computer abbreviations and acronyms section. 704 pages.

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An introductory textbook on calculators that reviews calculator capabilities, usage and programming from the basics of how to use keyboards, special function keys and preprogrammed units to advanced programmable calculator systems for use in engineering, science and communication. Includes a section on programming processes and procedures for calculators and a glossary of calculator terms.

1024 QUESTIONS AND ANSWERS ABOUT HOME COMPUTERS

Richard L. Didday

A book for the person interested in microcomputers who wants to get an idea of what it can be like before buying the equipment and for the person with a microcomputer who wants ideas for things to do, help in reading the literature, help in deciding what ways to go. 144 pages.



MATRIX PUBLISHERS, INC.

Dept. IF, 207 Kenyon Rd. Champaign, IL 61820

Matrix books also available in Byte Shops, computer stores, and bookstores.

CIRCLE INQUIRY NO. 11

Feb. 12 The Permian Basin Computer Group, Midland Chapter meets at 4:00 p.m., Midland College, Occupational Technology Bldg., Room 110, General Meeting. Call (915) 697-4697 for details.

Feb. 12 The Permian Basin Computer Group, Odessa Chapter meets at 1:00 p.m. Odessa College Electronics Technology Bldg., Room 203. Call (915) 332-9151 for more information.

Feb. 26 So. Cal. SWTPO MP 6800 Users Group meets at 10:00 a.m. at A-VID Electronics, 1655 E. 28th Street, Long Beach CA 70806.

Feb. 27 Chicago Area Computer Hobbyists Exchange (CACHE) meets at 12:00 noon, NIGAS Bldg., Schermer Rd., Glenview IL. Sick Computer Show. Bring in your problems and help repair them. Call Bill Precht at (312) 620-1671.

Feb. 28-Mar. 3 IEEE Computer Society's COMPCON '77 Spring beginning at 9:00 a.m. on Feb. 28 at the Jack Tar Hotel, San Francisco, California.

Mar. 2 New England Computer Society, Inc., meets at 7:00 p.m. MITRE Corp., Cafeteria, Route 62, Bedford, MA. General Meetings. Call Dave Day at (603) 434-4239.

Mar. 7 AMRAD Amateur Radio Research and Development Corp. meets at 8:00 p.m. in the Patrick Henry Library, Vienna, VA 22101. Call (703) 356-8918 for details.

March 9-11 DATACOMM '77 meets at Sheraton Park Hotel, Washington, DC. For more information contact Shaun Bresnahan, Director of Marketing, DATACOMM '77, 60 Austin St., Newtonville, MA 02160 or call (617) 964-4550.

Mar. 10 Rochester Area Microcomputer Society meets at 6:30 p.m. Room 1030, Bldg. 9, Rochester, NY. Mailing address, RAMS, P.O. Box D, Rochester NY 14609.

Mar. 22 So. Cal. SWTPO MP 6800 Users Group meets at 10:00 a.m. at A-VID Electronics, 1655 E. 28th Street, Long Beach, CA 70806.

Mar. 27 Chicago Area Computer Hobbyists Exchange (CACHE) meets at 12:00 noon, NIGAS Bldg., Schermer Rd., Glenview, IL. Small Business Opportunities Show. For further information contact Bill Precht at (312) 620-1671.

March 28-30 The 5th Annual Data Communications Conference and Exposition, INTERFACE '77 meets at Georgia World Congress Center, Atlanta, GA. For more information

contact Bob Goolta, INTERFACE, 160 Speen Street, Framingham, MA 01701

April 19-21 Electro/77 meets at New York Coliseum and Hotel Americana, New York, New York. For more information write Electro/77, 999 N. Sepulveda Blvd., El Segundo, CA 90245 or call (800) 421-6816.

May 10-12 Chicagoland Business Services and Equipment Exposition meets at ExpoCenter/Chicago. For further information contact Carleton Rogers, Industrial and Scientific Conference Management Inc., 222 West Adams St., Chicago, IL 60606 or call (312) 263-4866.

June 13-16 NCC, Dallas, TX. For more information write AFIPS, 210 Summit Ave., Montvale, NJ 07645 or call (201) 391-9810.

COMING IN MARCH ISSUE...

New Products Guide

The Computer Even a Baby Can Use

by Kenneth Perry, Basil Steele Rocky Ridges and Harry Garland

An informative glance at the future of microprocessors in medical applications

Reflections on the Past and Thoughts About the Future of Semiconductor Technology

by Dr. C. Lester Hogan
Dr. Hogan has earned the title "Father of Semi-conductor Technology." In *Reflections* this eminent scientist relates an engrossing travelogue of the arduous adventures encounter by him and his colleagues throughout the years of development of the technology.

The Menace of the Micro World

Another essay and program on artificial intelligence

The Qube by Roger Garrett
Science-fiction has such a provocative way of becoming science-fact

Building a Digital Group System

by Donald O. Southwick

More valuable information for our hardware readers

And for our software readers, programs on
Depreciation Schedule Analysis
Checkbook Balance
Game of Life
—and others



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... FROM THE FOUNTAINHEAD

By Adam Osborne

INTERFACE AGE I will bring you recent microprocessor and microcomputer happenings in the Northwest. I will concentrate on developments of technical interests rather than reviewing society meetings. The companies that I will cover include all of those between San Jose and San Francisco — an area known affectionately as Silicon Valley. To me this is the "fountain head" from which microprocessors flow, hence the title I have chosen for my column. Microprocessor manufacturers within this small area include Intel, National Semiconductor, Fairchild, Intersil, Signetics, Scientific Micro Systems, Advanced Micro Devices, American Microsystems, Advanced Memory Systems, Electronic Arrays, Zilog and Synertek. Microcomputer manufacturers include IMSAI, Processor Technology, Cromemco, and Apple — and the Byte shops began here. These are the types of companies whose activities I will cover.

If you have information about your company about which you would like me to write, or if you have comments about what I have written, please call me directly at (415) 548-2805.

And now for some recent happenings of interest.

Guess who will sell the most 8-bit microprocessors in 1977? Intel with the 8080? Wrong! Fairchild with the F8 will outsell the 8080 at least 2-to-1 — providing Fairchild can manufacture enough product to fill orders. Yes, Fairchild is currently production bound. Fairchild has orders for between two million and three million F8 microprocessors in 1977.

But that is not very interesting to the low volume user because Fairchild's customer base consists of a few, very high volume accounts. Low volume and individual users don't take too readily to the F8.

Zilog is doing deceptively well. They are currently shipping approximately 5,000 CPUs a month. That does not sound like many when stacked up against 8080 or F8 sales, but numbers can be misleading. Big sales volume doesn't come until manufacturers put the Z80 into something that sells tens of thousands of units monthly. Typically it takes two years for a big user to bring a product with such large sales volume to the market. All those guys who will be buying 10,000 Z80 CPUs a month, now are buying 5 or 10 at a time. Zilog's present customer base suggests that Zilog will be selling many Z80's in 1979. Exxon be patient.

Intel's answer to the Z80, the 8085, is finally here. Is it a mouse or a powerhouse? It has the same instruction set as the 8080A, with just two additional I/O instructions — but it uses a single power supply and condenses the 8080A, 8224 and 8228 into a single chip. But the 8085 address and data

buses are multiplexed. When Intel went from the 8008 to the 8080 I thought one of the big advances was to get rid of multiplex data and address buses.

The 8048 is Intel's answer to the F8. It is a single chip microcomputer, complete with CPU, interrupt logic, ROM, RAM, and I/O. The 8748 is a version with erasable ROM and that should make the chip the darling of all small manufacturers.

Fairchild cannot make erasable ROMs so they are coming up with a 40 pin package that combines the new, one chip 3859 F8 microcomputer with external erasable ROM. If the price is right, so is the product.

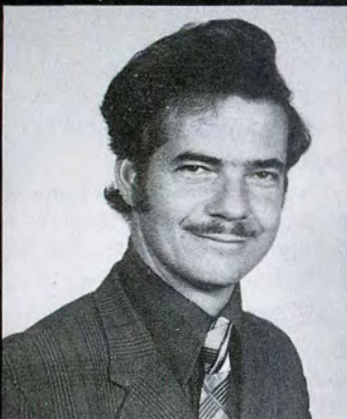
For all of you 8080A users who are into hardware, Advanced Micro Devices is coming out with a book which you must buy. It is packed with all kinds of good design tips. Contact Andrew Allison or Joe Kroeger for details. And plan on spending some money; the book costs \$10 but it is worth the price.

Some big names are impressed enough with the microcomputer hobby market to jump on the band wagon. Pertec has bought MITS, the father of the Altair and the hobby market, and iCOM who built the first floppy disk drive to interface with microprocessors. iCOM uses Pertec floppy disk drives so Pertec is simply buying its best customer. But did you know that when the guys who started iCOM first went to Pertec to buy drives, they had to pay cash on the barrel head? Pertec thought they were too flaky for credit. Eighteen months later Pertec bought them for a quarter of a million Pertec shares. Not bad for 18 months' work.

But that is not the only Pertec story. Stu Mabon, Eric Dunstan, et. al started Pertec in a garage, back in 1968. Stu Mabon, Eric Dunstan, et. al. have quit Pertec and have started another new company. Wait for those guys to announce some big floppy disk breakthroughs in the next three months.

Have you heard the rumors about Heath Kit getting into the microcomputer hobby market? They are all true. Starting late this summer the Heath Company will be marketing a very well known, big name microcomputer system at a low, low price. And won't it be nice to have Heath Kit quality documentation to work from for a change?

How will all of the other retail outlets react to Heath Kit? Those with multiple lines will make it. Any retail store that markets just one microcomputer is severely handicapped in competition with retail outlets such as the Byte Shops which carry multiple lines. After all, what successful stereo and sound system stores try to sell just one line? I predict that the stores marketing just one microcomputer line will diversify or go under.



Let me introduce myself, I am Adam Osborne. Starting with this issue of *INTERFACE AGE*, I will be the Northwest regional editor. In every issue of

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8080 OCTAL MONITOR PROGRAM

By Thomas E. Doyle

INTRODUCTION

This monitor program will enable you to control your 8080 system from an ASCII keyboard and a TTY or CRT readout. All standard front panel control functions (examine, examine next, deposit, load and run) are provided in octal format. Audio cassette input and output functions as well as a loader for MITS software are also included. Once you have this monitor in ROM, the drudgery of entering and reading data from the front panel switches and lights is all but eliminated.

PORT ASSIGNMENTS

The monitor is designed to operate in an 8080 system with keyboard data input on port 1 and keyboard data available checked on port 0, LSB (active low). Data output is also available on port 1 with terminal ready to receive data checked on port 0, MSB (active low). The audio cassette interface data are on port 7 with status checked on port 6. These standards correspond with MITS port assignments used for the ACR and serial I/O boards used in Basic and Package II software.

MEMORY REQUIREMENTS

Required are 512 bytes of memory which may be ROM or RAM. The program may be located anywhere in memory. A source object listing assembled to start at 376 000 is included at end of text. The best configuration is to put the monitor in EROM and locate it in a high memory location so it may reside concurrently with programs in the low RAM address. The program is organized as a series of general purpose subroutines which may be called from user programs.

MONITOR FUNCTION

The monitor functions are:

EXAMINE (E)	User types in octal address of memory location he wishes to examine and the computer prints out the address and data in octal format. HHH LLL : DDD :
EXAMINE NEXT	(SPACE) When in the <i>examine</i> mode the user may type the space bar and the computer will print the address and data for the next location in memory in octal format. HHH LLL : DDD :
DEPOSIT (D)	After examining a location the user may deposit new data in that location by typing the letter D followed by the new data in octal format. The computer checks for proper storage by typing out the octal equivalent of the data actually stored at that address. HHH LLL : DDD : D XXX XXX

Where XXX is the new octal data the user wishes to deposit at the address.

Note: You must examine a location before you can deposit data in that location.

RUN (R)	After examining a location the user may elect to start program execution at that address by typ-
---------	--

ing the letter R.

Note: you must examine a location before you can begin program execution at that location.

LOAD (L)

After examining a location the user may elect to load octal data in sequential addresses by typing in L followed by the octal data. After the third digit in each octal number the computer will deposit the data in that address and check it as in the *deposit* mode, increment the address and automatically accept the next octal number. This mode is useful when you have a large amount of data to enter in sequential locations.

Note: You must examine the starting address before you can begin loading.

TAPE OUTPUT

Typing an O will select the tape output mode. The Computer will ask for the starting and ending addresses for the block of data you wish to put on cassette tape. After typing in the start and finish addresses, type space to begin output. The computer will record two STX characters (002) followed by the data. When it is finished the terminal will print: indicating it is through outputting data to the tape and is ready for a new command.

TAPE INPUT (I)

Typing an I will select the tape input mode. The computer will ask for the starting address where you wish to begin depositing the data from the cassette tape. Type a space following the address. When you are through entering the tape, type in a carriage return and the computer will print a : indicating it is ready for a new command.

Note: the system will not automatically return to command mode at the end of the tape. You must type carriage return.

BOOT STRAP (B)

Typing a B will copy a modified MITS cassette boot strap loader for 8K Basic down into RAM starting at location 000 000. After typing B, type a space and start your basic tape. No need to wait the 15 seconds. This feature will be greatly appreciated by those who have grown weary of toggle switching the boot strap in. Since the boot strap is copied into RAM you may make any necessary changes before starting execution.

Note: Typing a carriage return will return the monitor

to the command mode.

SUBROUTINES AVAILABLE FOR USER APPLICATIONS

Several of the subroutines used in the monitor may be used to handle I/O in user programs. These subroutines save all used registers so it is only necessary to call the subroutines.

PNT: Prints the contents of the accumulator on the terminal connected to port 1.

INP: Inputs data from the keyboard and returns with the data in the accumulator. The routine INP (page 2 000) is not used in the program. It is a general purpose routine for input from a keyboard and returning with the keyboard data in the accumulator. It was included as a general purpose routine for use in other programs.

CRL: Outputs an ASCII carriage return and linefeed.

SPC: Outputs an ASCII space.

POC: Prints the octal equivalent of the accumulator contents.

IOC: Inputs a 3 digit octal number from the keyboard and returns with data in accumulator.

TOT: Outputs the contents of the accumulator to the audio cassette interface.

TIN: Inputs from the audio cassette interface and returns with the data in the accumulator.

PROGRAM EXPANSION

Provision for simple expansion of the program is provided for by including a group of 3 NO-OPS in two critical locations. The end of the print (PNT) subroutine contains 3 NOP's which may be used for a call to a special I/O handler program (i.e. ASCII to BAUDOT converter). The input control (INC) subroutines inputs from the keyboard and runs through a series of comparisons to determine which command is present. If the program reaches the bottom of the list of comparisons without finding a match it enters a default routine which prints a ? indicating that an invalid command was present. Three NO - OPS are included just ahead of the default routine to allow calling another set of comparisons and associated jumps for additional commands.

This monitor is by no means the ultimate but it does provide all basic control of the microcomputer and I/O. The length was arbitrarily limited to 512 bytes so it could be held on two 1702 type PROMS. Possible areas for expansion are:

- Tape verify routine, after a block of memory has been recorded on audio cassette it could be read in and verified.
- HEX format, basic monitor functions handled in HEX format.
- Cassette I/O improvements, inclusion of file names and checksum on input and output routines.

NOTES ON MODIFIED MITS BOOTSTRAP LOADER

This routine copies the modified bootstrap loader, which is stored in the monitor program starting at (page 2 016), down to RAM starting at (000 000). After the routine has been copied down the routine waits for a key to be pressed on the keyboard. If any key other than a carriage return is pressed program execution will begin at the start of the bootstrap (000 024). The loader that is copied down is for MITS 8K BASIC version 3.2.

If you wish to load software other than 8K BASIC, after typing B type a carriage return. You will now be back in the command mode and you can change what

ever you need to by changing memory location (000 002) to 017 for 4-K Basic and Programming System II or to 057 for EXTENDED BASIC in the bootstrap. After making the changes, begin execution at (000 024).

The routine waits for the correct character marking the beginning of MITS tapes (Memory page 2 Address 044). For most current software this is 256. If you have an old version change location (000 027) to what ever character starts your tape. (Some older tapes use 175)

NOTES ON LISTING

The Program is contained on two 256 word pages. The first page contains the instructions for the commands. The second page contains the general purpose subroutines. The two pages do not have to be adjacent in memory. The listing includes object code for page 1 with a high address of 376 and page 2 with a high address of 377. These page references are underlined in the listing. Changing these page references in the jump and call commands will allow the program to run in any two blocks of memory, location of the stack

The first instruction (376 000) sets the stack pointer. Location of the stack pointer is dependent upon user's ram configuration and may be changed depending on your available memory.

PORT ASSIGNMENTS MAY BE CHANGED BY CHANGING

(PAGE 2 346) FOR KEYBOARD STATUS
(PAGE 2 354) FOR KEYBOARD DATA
(PAGE 2 364) FOR DISPLAY STATUS
(PAGE 2 373) FOR DISPLAY DATA
(PAGE 2 116) AND (PAGE 2 136) FOR ACR BOARD STATUS
(PAGE 2 125) AND (PAGE 2 146) FOR ACR BOARD DATA
PROGRAM EXECUTION BEGINS AT (PAGE 1 000)

COMMAND PROCESSING

MEMORY PAGE 1		
000-061 377 037	INC: LXI SP	:LOAD STACK POINTER
003-315 302 377	STA: CALL CLC	:PRINT CR/LF AND :
006-315 345 377	CALL RCV	:INPUT KEYBOARD DATA
011-376 105	CPI "E"	:COMPARE FOR ASCII "E"
013-312 050 376	JZ EXA	:JUMP TO EXAMINE ROUTINE IF "E"
016-376 111	CPI "I"	:COMPARE ASCII "I"
020-312 202 376	JZ TIP	:JUMP TO TAPE INPUT IF "I"
023-376 117	CPI "O"	:COMPARE FOR ASCII "O"
025-312 246 376	JZ TOD	:JUMP TO TAPE OUTPUT IF "O"
030-376 102	CPI "B"	:COMPARE FOR ASCII "B"
032-312 345 376	JZ BSL	:JUMP TO BOOT LOADER IF "B"
035-000	NOP	:GROUP OF THREE NO OPS TO
036-000	NOP	:ALLOW EXPANSION OF
037-000	NOP	:COMMAND TABLE
040-076 077	DEF: MVIA, "?"	:MOVE ASCII "?" TO A
042-315 362 377	CALL PNT	:CALL PRINT SUBROUTINE
045-303 003 376	JMP STA	:JUMP BACK TO START

EXAMINE

050-315 315 377	EXA: CALL CL>	:PRINT CR/LF AND>
053-315 150 377	CALL LHK	:LOAD H AND L FROM OCTAL INPUT FROM KEYBOARD
056-315 330 377	PXA: CALL CRL	:PRINT CR/LF
061-315 166 377	CALL POH	:PRINT OCTAL ADDRESS AND DATA
064-076 072	MVIA, "?"	:MOVE ASCII "?" TO A
066-315 362 377	CALL PNT	:CALL PRINT SUBROUTINE
071-315 345 377	CALL RCV	:INPUT DATA FROM KEYBOARD
074-376 040	CPI " "	:COMPARE ASCII "SPACE"
076-312 123 376	JZ EXN	:JUMP TO EXAMINE NEXT IF "SPACE"
101-376 122	CPI "R"	:COMPARE ASCII "R"
103-312 127 376	JZ RUN	:JUMP TO RUN IF "R"
106-376 104	CPI "D"	:COMPARE ASCII "D"
110-312 130 376	JZ DEP	:JUMP TO DEPOSIT IF "D"
113-376 114	CPI "L"	:COMPARE ASCII "L"
115-312 152 376	JZ LDE	:JUMP TO LOAD IF "L"
120-303 040 376	JMP DEF	:JUMP TO DEFAULT ROUTINE

EXAMINE NEXT

123-043	EXN: INX H	:INCREMENT H AND L
124-303 056 376	JMP PXA	:JUMP TO PRINT OCTAL ADDRESS AND DATA

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CIRCLE INQUIRY NO. 16

RUN

127-351 RUN:PCHL :START EXECUTION AT ADDRESS REFERENCED BY H AND L
124-303 056 376 JMP PXA :JUMP TO PRINT OCTAL ADDRESS AND DATA

RUN

127-351 RUN:PCHL :START EXECUTION AT ADDRESS REFERENCED BY H AND L

DEPOSIT

130-315 272 377 DEP:CALL SPC :CALL PRINT SPACE SUBROUTINE
133-315 054 377 CALL OCI :CALL OCTAL DATA IN FROM KEYBOARD
136-167 MOV M.A :STORE DATA IN MEMORY
137-315 272 377 CALL SPC :PRINT SPACE
142-176 MOV A.M :MOVE DATA FROM MEMORY TO A
143-315 231 377 CALL POC :PRINT OCTAL EQUIVALENT OF DATA
146-043 INX H :INCREMENT H AND L
147-303 056 376 JMP PXA :JUMP TO PRINT OCTAL ADDRESS AND DATA

LOAD

152-315 330 377 LDE:CALL CRL :PRINT CARRIAGE RETURN/LINE FEED
155-315 166 377 CALL POH :PRINT OCTAL EQUIVALENT OF ADDRESS AND DATA
160-315 272 377 CALL SPC :PRINT ASCII "SPACE"
163-315 054 377 CALL OCI :LOAD OCTAL DATA FROM KEYBOARD
166-167 MOV M.A :MOVE DATA TO MEMORY
167-315 272 377 CALL SPC :PRINT ASCII "SPACE"
172-176 MOV A.M :MOVE DATA FROM MEMORY
173-315 231 377 CALL POC :PRINT OCTAL EQUIVALENT OF DATA
176-043 INX H :INCREMENT H AND L
177-303 152 376 JMP LDE :JUMP FOR NEXT BYTE

TAPE IN

202-315 315 377 TIP: CALL CL> :PRINT CR/LF AND<
205-315 150 377 CALL LHK :LOAD H AND L FROM KEYBOARD
210-315 302 377 CALL CLC :PRINT CR/LF AND<
213-315 345 377 CALL RCV :WAIT FOR A KEY ON KEYBOARD TO BE DEPRESSED
216-315 127 377 TSC:CALL TIN :INPUT DATA FROM ACR BOARD
221-376 002 CPI "2" :CHECK FOR STX (002)
223-302 216 376 JNZ TSC :JUMP IF DATA IS NOT STX
226-315 127 377 TSD:CALL TIN :INPUT DATA FROM ACR BOARD
231-376 002 CPI "2" :CHECK FOR STX (002)
233-302 226 376 JNZ TSD :JUMP IF DATA IS NOT STX
236-315 127 377 TSN:CALL TIN :INPUT DATA FROM ACR BOARD
241-167 MOV M.A :STORE DATA
242-043 INX H :INCREMENT H AND L
243-303 236 376 JMP TSN :JUMP FOR NEXT BYTE

TAPE OUT

246-315 315 377 TOD:CALL CL> :PRINT CR/LF AND<
251-315 150 377 CALL LHK :LOAD H AND L FROM KEYBOARD
254-315 272 377 CALL SPC :PRINT SPACE
257-076 124 MVI A, "T" :MOVE ASCII T TO ACCUMULATOR
261-315 362 377 CALL PNT :PRINT T
264-076 117 MVI A, "O" :MOVE ASCII O TO ACCUMULATOR
266-315 362 377 CALL PNT :PRINT O
271-315 272 377 CALL SPC :PRINT A SPACE
274-345 PUSH H :PUSH H AND L
275-315 150 377 CALL LHK :LOAD H AND L FROM KEYBOARD
300-124 MOV D, H :MOVE H TO D
301-135 MOV E, L :MOVE L TO E
302-341 POP H :POP H AND L
303-315 330 377 CALL CRL :PRINT CR/LF
306-076 002 MVI A, "2" :MOVE STX "002" TO ACCUMULATOR
310-315 113 377 CALL TOT :RECORD STX ON TAPE
313-076 002 MVI A, "2" :MOVE STX "002" TO ACCUMULATOR
315-315 113 377 CALL TOT :RECORD STX ON TAPE
320-176 TOE:MOV A, M :MOVE DATA FROM MEMORY TO ACCUMULATOR
321-315 113 377 CALL TOT :RECORD DATA ON TAPE
324-174 MOV A, H :MOVE H TO A
325-272 CMP D :COMPARE D WITH H
326-302 341 376 JNZ TON :JUMP IF D NOT = H
331-175 MOV A, L :MOVE L TO A
332-273 CMP E :COMPARE E WITH L
333-302 341 376 JNZ TON :JUMP IF E NOT = L
336-303 003 376 JMP STA :JUMP BACK TO MONITOR SINCE ENTIRE BLOCK HAS BEEN RECORDED
341-043 TON:INX H :INCREMENT H AND L
342-303 320 376 JMP TOE :JUMP FOR NEXT BYTE

MITS BOOTSTRAP

345-021 000 000 BSL:LXI D, "0,0" :LOAD D AND E WITH 000 000
350-041 016 377 LXI H, "377 016" :LOAD H AND L WITH 376 016
353-176 MOV A, M :MOVE M TO A
354-353 BSN:XCHG :EXCHANGE H AND L WITH D AND E
355-167 MOV M, A :STORE DATA
356-353 XCHG :EXCHANGE H AND L WITH D AND E
357-175 MOV A, L :MOVE L TO A
360-376 055 CPI "055" :CHECK FOR END
362-312 372 376 JZ END :JUMP IF END
365-043 INX H :INCREMENT H AND L
366-023 INX D :INCREMENT D AND E
367-303 353 376 JMP BSN :JUMP FOR NEXT BYTE
372-315 345 377 END:CALL RCV :WAIT FOR KEY ON KEYBOARD TO BE DEPRESSED
375-303 024 000 JMP "000 024" :JUMP TO 000 024 WHICH IS START OF BOOTSTRAP LOADER PROGRAM
000-333 000 INP: INO :INPUT KEYBOARD STATUS
002-017 RRC :ROTATE RIGHT
003-332 000 377 JCINP :JUMP BACK IF NO DATA AVAILABLE
006-333 001 IN 1 :INPUT KEYBOARD DATA
010-000 NOP :NO OPERATION
011-000 NOP :NO OPERATION
012-000 NOP :NO OPERATION
013-303 362 377 JMP PNT :JUMP TO PRINT SUBROUTINE
016-041 256 037 BSP LXI H :LOAD H AND L WITH (037 256)
021-061 022 000 LXI SP :LOAD STACK POINTER WITH (000 022)
024-333 006 IN 6 :INPUT ACR STATUS
026-017 RRC :ROTATE RIGHT
027-330 RC :ROTATE IF CARRY
030-333 007 IN 7 :INPUT ACR DATA
032-275 CMP L :COMPARE L
033-310 RZ :RETURN IF ZERO
034-055 DCR L :DECREMENT L
035-167 MOV M, A :MOVE DATA TO MEMORY
036-300 RNZ :RETURN IF NOT ZERO
037-351 PCH L :EXCHANGE PC WITH H AND L
040-003 INX B :INCREMENT B AND C
041-000 NOP :NO OPERATION
042-333 007 IN 7 :INPUT ACR DATA
044-376 256 CPI 256 :COMPARE FOR CHARACTER MARKING 256
046-302 024 000 JNZ (000 024) :JUMP BACK IF DATA IS NOT 256
051-303 000 000 JMP (000 000) :JUMP TO START OF BOOTSTRAP
054-305 OCF: PUSH B :PUSH B
055-006 000 MVI B :MOVE 000 TO B
057-315 345 377 CALL RCV :CALL KEYBOARD DATA INPUT
062-346 003 ANI "3" :AND IMMEDIATE (MASK 2 LSB'S)

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065-037	RAR	:THREE TIMES
066-037	RAR	:
067-200	ADD B	:ADD B
070-107	MOV B.A	:MOVE A TO B
071-315 345 377	CALL RCV	:CALL KEYBOARD DATA INPUT
074-346 007	ANI "7"	:AND IMMEDIATE (MASK 3 LSB'S)
076-007	RLC	:ROTATE LEFT THROUGH
077-007	RLC	:CARRY THREE
100-007	RLC	:TIMES
101-200	ADD B	:ADD B
102-107	MOV B.A	:MOVE A TO B
103-315 345 377	CALL RCV	:CALL KEYBOARD DATA INPUT
106-346 007	ANI "7"	:AND IMMEDIATE (MASK 3 LSB'S)
110-200	ADD B	:ADD B
111-301	POP B	:POP B AND C REGISTERS
112-311	RET	:UNCONDITIONAL RETURN
113-365	TOT: PUSH PSW	:PUSH ACCUMULATOR
114-067	STC	:SET CARRY
115-333 006	TOI: IN 6	:INPUT ACR BOARD STATUS
117-007	RLC	:ROTATE LEFT THROUGH CARRY
120-332 115 377	JC TOI	:JUMP IF VART BUFFER FULL
123-361	POP PSW	:POP ACCUMULATOR
124-323 007	OUT 7	:OUTPUT DATA TO ACR BOARD
126-311	RET	:UNCONDITIONAL RETURN
127-333 001	TIN: IN 1	:INPUT KEYBOARD DATA
131-376 015	CPI "CR"	:COMPARE FOR ASCII CARRIAGE RETURN
133-312 003 376	JZ STA	:JUMP IF ASCII CARRIAGE RETURN
136-067	STC	:SET CARRY BIT
137-333 006	IN 6	:INPUT ACR BOARD STATUS
141-017	RRC	:ROTATE RIGHT THROUGH CARRY
142-332 127 377	JC TIN	:JUMP IF NO DATA AVAILABLE
145-333 007	IN 7	:INPUT ACR BOARD DATA
147-311	RET	:UNCONDITIONAL RETURN
150-365	LHK: PUSH PSW	:PUSH ACCUMULATOR
151-315 054 377	CALL OCI	:CALL OCTAL IN
154-147	MOV H.A	:MOVE ACCUMULATOR TO H
155-315 272 377	CALL SPC	:PRINT A SPACE
160-315 054 377	CALL OCI	:CALL OCTAL INPUT
163-157	MOV L.A	:MOVE ACCUMULATOR TO L
164-361	POP PSW	:POP ACCUMULATOR
165-311	RET	:UNCONDITIONAL RETURN
166-365	POH: PUSH PSW	:PUSH ACCUMULATOR
167-315 204 377	CALL POA	:PRINT OCTAL EQUIVALENT OF ADDRESS
172-076 072	MVIA, "H"	:MOVE ASCII H TO ACCUMULATOR
174-315 362 377	CALL PNT	:PRINT :
177-315 222 377	CALL POD	:PRINT OCTAL EQUIVALENT OF DATA
202-361	POP PSW	:POP ACCUMULATOR
203-311	RET	:UNCONDITIONAL RETURN
204-365	POA: PUSH PSW	:PUSH ACCUMULATOR
205-174	MOV A.H	:MOVE H REGISTER TO ACCUMULATOR
206-315 231 377	CALL POC	:PRINT OCTAL EQUIVALENT OF H REGISTER
211-315 272 377	CALL SPC	:PRINT A SPACE
214-175	MOV A.L	:MOVE L REGISTER TO ACCUMULATOR
215-315 231 377	CALL POC	:PRINT OCTAL EQUIVALENT OF L REGISTER
220-361	POP PSW	:POP ACCUMULATOR
221-311	RET	:UNCONDITIONAL RETURN
222-365	POD: PUSH PSW	:PUSH ACCUMULATOR
223-176	MOV A.M	:MOVE MEMORY DATA TO ACCUMULATOR
224-315 231 377	CALL POC	:PRINT ACCUMULATOR OCTAL EQUIVALENT
227-361	POP PSW	:POP ACCUMULATOR
230-311	RET	:UNCONDITIONAL RETURN
231-345	POC: PUSH H	:PUSH H AND L REGISTERS
232-157	MOV L.A	:MOVE ACCUMULATOR TO L
233-007	RLC	:ROTATE LEFT TWICE
234-007	RLC	:
235-346 003	ANI "3"	:MASK OFF ALL BUT 3 BITS
237-366 260	ORI 260	:FORM ASCII DIGIT
241-315 362 377	CALL PNT	:PRINT FIRST OCTAL DIGIT
244-175	MOV A.L	:MOVE L TO ACCUMULATOR
245-017	RRC	:ROTATE RIGHT 3 TIMES
246-017	RRC	:
247-017	RRC	:
250-346 007	ANI "7"	:MASK OFF ALL BUT 3 BITS
252-366 260	ORI 260	:FORM ASCII DIGIT
254-315 362 377	CALL PNT	:PRINT SECOND OCTAL DIGIT
257-175	MOV A.L	:MOVE L TO ACCUMULATOR
260-346 007	ANI "7"	:MASK OFF ALL BUT 3 BITS
262-366 260	ORI 260	:FORM ASCII DIGIT
264-315 362 377	CALL PNT	:PRINT THIRD OCTAL DIGIT
267-175	MOV A.L	:MOVE L TO ACCUMULATOR
270-341	POP H	:POP H AND L REGISTERS
271-311	RET	:UNCONDITIONAL RETURN
272-365	SPC: PUSH PSW	:PUSH ACCUMULATOR
273-076 040	MVI A, " "	:MOVE ASCII SPACE TO ACCUMULATOR
275-315 362 377	CALL PNT	:PRINT SPACE
300-361	POP PSW	:POP PSW
301-311	RET	:UNCONDITIONAL RETURN
302-365	CLC: PUSH PSW	:PUSH ACCUMULATOR
303-315 330 377	CALL CRL	:PRINT CARRIAGE RETURN AND LINE FEED
306-076 072	MVIA, "H"	:MOVE ASCII H TO ACCUMULATOR
310-315 362 377	CALL PNT	:PRINT :
313-361	POP PSW	:POP ACCUMULATOR
314-311	RET	:UNCONDITIONAL RETURN
315-365	CLC: PUSH PSW	:PUSH ACCUMULATOR
316-315 330 377	CALL CRL	:PRINT CARRIAGE RETURN AND LINE FEED
321-076 076	MVIA, ">"	:MOVE ASCII > TO ACCUMULATOR
323-315 362 377	CALL PNT	:PRINT
326-361	POP PSW	:POP ACCUMULATOR
327-311	RET	:UNCONDITIONAL RETURN
330-365	CRL: PUSH PSW	:PUSH ACCUMULATOR
331-076 015	MVI A, "CR"	:MOVE ASCII CARRIAGE RETURN TO ACCUMULATOR
333-315 362 377	CALL PNT	:PRINT CARRIAGE RETURN
336-076 012	MVIA, "LF"	:MOVE ASCII LINE FEED TO ACCUM
340-315 362 377	CALL PNT	:PRINT LINE FEED
343-361	POP PSW	:POP ACCUMULATOR
344-311	RET	:UNCONDITIONAL RETURN
345-333 000	RCV: IN 0	:INPUT STATUS CHANNEL
347-017	RRC	:CHECK LSB
350-332 345 377	JC RCV	:JUMP BACK IF NO KEYBOARD DATA
353-333 001	IN 1	:INPUT KEYBOARD DATA
355-376 015	CPI "CR"	:COMPARE FOR ASCII CARRIAGE RETURN
357-312 003 376	JZ "STA"	:JUMP TO START IF CARRIAGE RETURN
362-365	PNT: PUSH PSW	:PUSH ACCUMULATOR
363-333 000	PNA: IN 0	:INPUT STATUS CHANNEL
365-007	RLC	:CHECK MSB
366-332 363 377	JC PNA	:JUMP BACK IF TERMINAL NOT READY
371-361	POP PSW	:POP ACCUMULATOR
372-323 001	OUT 1	:PRINT ACCUMULATOR CONTENTS
374-000	NOP	:NO-OPS TO ALLOW CALL TO
375-000	NOP	:SPECIAL I/O HANDLER
376-000	NOP	:ROUTINE
377-311	RET	:UNCONDITIONAL RETURN

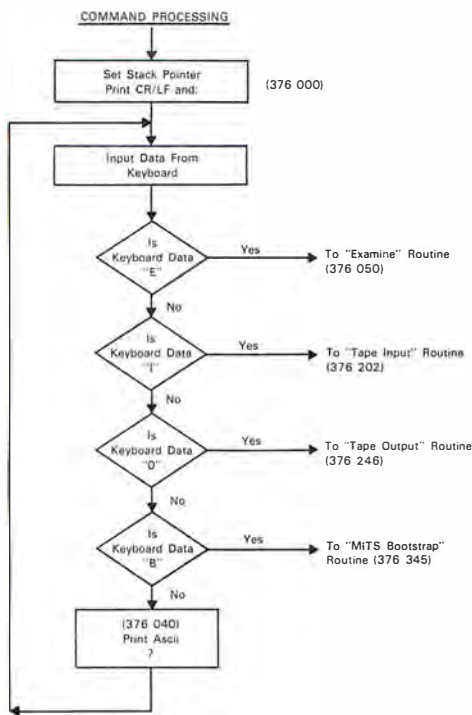


Figure 1.

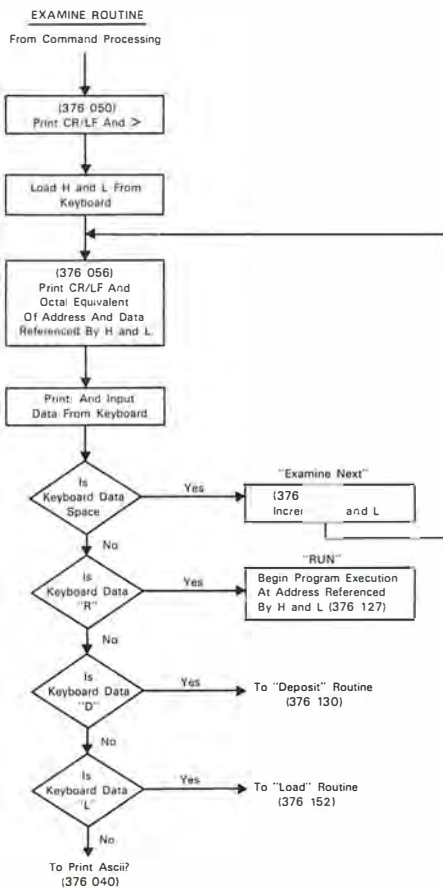


Figure 2

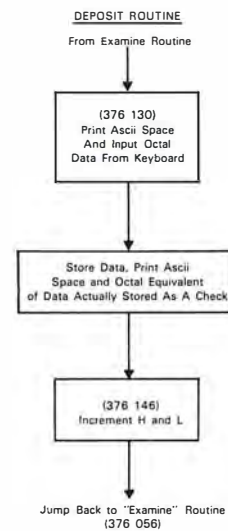
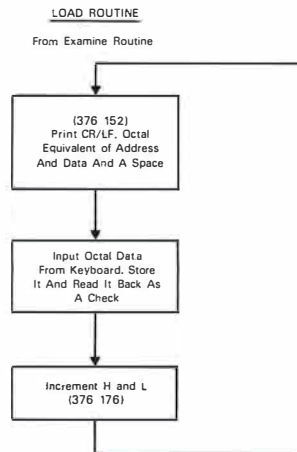
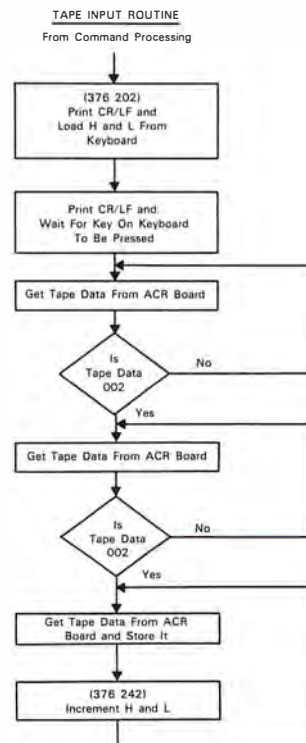


Figure 3.



NOTE: Typing a carriage return instead of octal data will cause a return to the command process routine.

Figure 4.



NOTE: After the tape has been read in, type a carriage return to return to the command process routine.

Figure 5.

PRAMMER by Xybek



★ **1702A PROM PROGRAMMER, 1792 bytes of 1702A EPROM, and 256 bytes of RAM, all on one board.** The programmer is not an I/O device. At the flick of a switch, one of the 1702A positions becomes a programming address. With programming enabled, storing into this address space will program the PROM. With programming disabled, that address space is just ordinary read-only memory.

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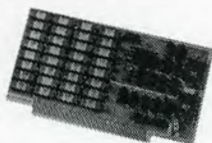
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CIRCLE INQUIRY NO. 21

TAPE OUTPUT ROUTINE

From Command Processing

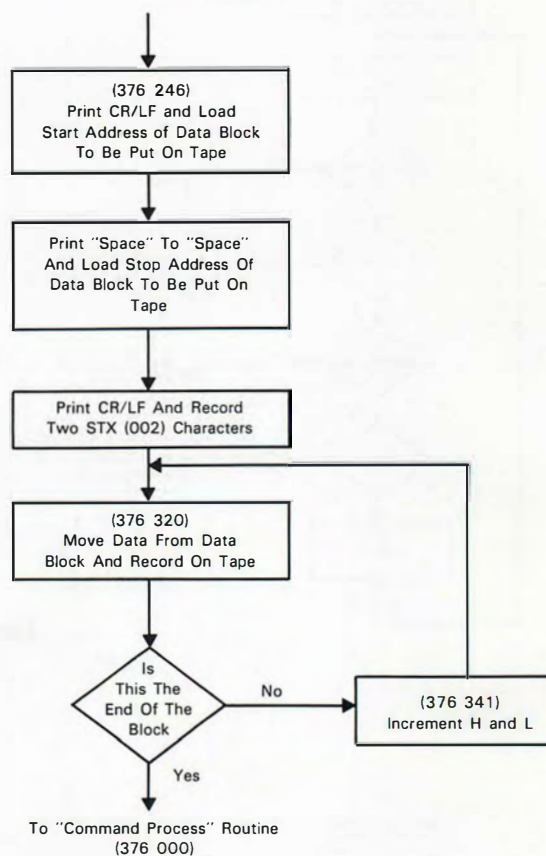


Figure 6.

MODIFIED MITS BOOTSTRAP

From Command Processing

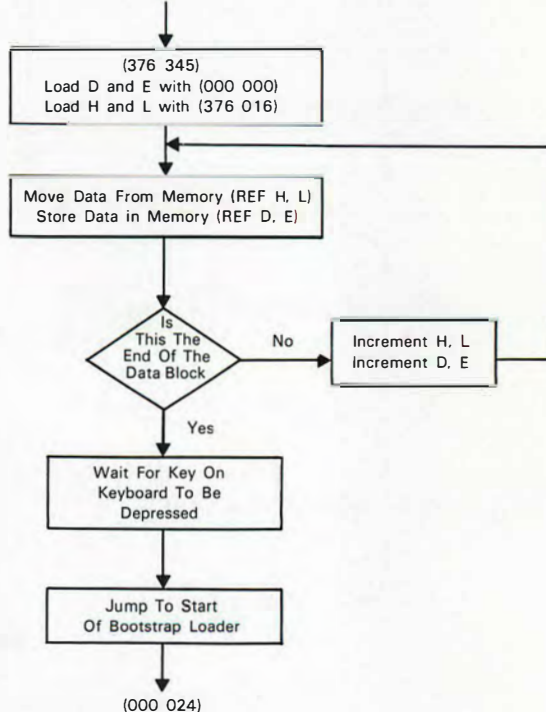


Figure 7.

DIGITAL DATA RECORDERS

USING 3M DATA CARTRIDGES



MODEL 3M3 \$199.95

(Price Increases to \$220.00 effective 1 April 77)

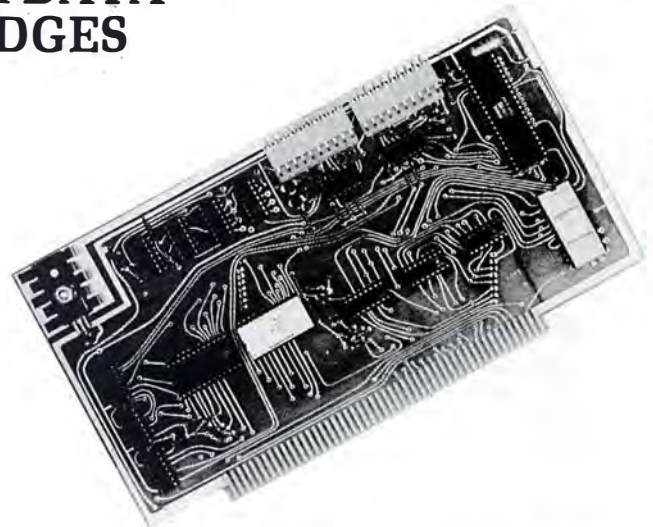
MODEL 3M3 Featuring the radically new "Uniboard" method of construction for data cartridge drives. The major computer makers are changing to cartridges at a rapid pace because of the freedom from binding and greater data reliability. Operates in the phase encoded self-clocking mode which provides greatly enhanced freedom from speed variation problems and allows 100% tape interchangeability between units.

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Specifications: Full software control of record, play, fast forward and rewind. LED indicates inter-record gaps. EOT and BOT are sensed and automatically shut down recorder. Feedback signals send reset and inter-record gap signals back to the computer so that software searching for inter-record gaps at high speed can be accomplished. Can also be operated manually by means of the switches on top which parallel the software control signals. \$199.95 until April 1, 77. \$220.00 after April 1, 77. Includes Phase Encoder Board (ACI).

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\$160, Kit form.

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In sharp contrast, a logic designer who is using a microcomputer to replace combinatorial logic must look upon programming and digital logic as two interdependent aspects of microprocessor utilization.

Most microprocessor courses being taught at the present time do not accurately stress the interdependence of hardware and software. The student can go through an assembly language programming course, and the fact that a microcomputer assembly language has been taught leaves the student no closer to understanding how the microprocessor should be used. Unless assembly language is taught as an alternative to implementing transfer functions which could otherwise be implemented using combinatorial logic, students will not understand how to use microprocessors in a digital logic environment. The purpose of the course being taught by Osborne & Associates is to provide this direct comparison between hardware and programming. Students attending our course are taught how to decide whether hardware or instructions within a microcomputer system should be used in order to implement each step of any product. Emphasis is placed on giving the student a flexible understanding of whether to keep logic inside or outside the microcomputer system, how to configure the microcomputer system, and how to write programs that drive the configured microcomputer system.

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8:30 - 10:00 a.m.	SESSION 1 Single Signal Logic	SESSION 4 The Central Processing Unit	SESSION 7 Assembly Language Programming	SESSION 9 Subroutines and Interrupts	SESSION 11 Parallel Interfaces
BREAK					
10:30 a.m. - 12:00	SESSION 2 Parallel Data Concepts	SESSION 5 Memory Organization	SESSION 8 Memory Addressing Modes	SESSION 10 The 8080A CPU	SESSION 12 Serial I/O
LUNCH					
1:00 - 2:30 p.m.	SESSION 3 The Structure Of A Microcomputer	SESSION 6 Elementary Assembly Language Programming	HANDOUT 4	HANDOUT 4 (Cont'd) HANDOUT 5	HANDOUT 5 (Cont'd)
BREAK					
3:00 - 4:30 p.m.	HANDOUT 1/HANDOUT 2	HANDOUT 3	HANDOUT 4 (Cont'd)	HANDOUT 5 (Cont'd)	HANDOUT 5 (Cont'd)
EVENING					
	HANDOUT 1/HANDOUT 2 (Cont'd)	HANDOUT 3 (Cont'd)	HANDOUT 4 (Cont'd)	HANDOUT 5 (Cont'd)	HANDOUT 5 (Cont'd) HANDOUT 6
TIME	DAY 6	DAY 7	DAY 8	DAY 9	DAY 10
8:30 - 10:00 a.m.	SESSION 13 Memory Systems Configurations	SESSION 15 Programming Aspects Of Interrupts	SESSION 17 The Theory Of Direct Memory Access	COMPLETE HANDOUTS	An Overview of Microcomputer Systems
BREAK					
10:30 - 12:00	SESSION 14 One-Shots & Interval Timing: The 8253 Programmable Timer	SESSION 16 Interrupt Handling Devices	SESSION 18 The 8257 Direct Memory Access Controller	COMPLETE HANDOUTS	An Overview Of Microcomputer Systems (Cont'd)
LUNCH					
1:00 - 2:30 p.m.	HANDOUT 6 (Cont'd) HANDOUTS 7, 8 & 9	SESSION 16 (Cont'd)	COMPLETE HANDOUTS	COMPLETE HANDOUTS	An Overview Of Microcomputer Systems (Cont'd)
BREAK					
3:00 - 4:30 p.m.	COMPLETE HANDOUTS	COMPLETE HANDOUTS	COMPLETE HANDOUTS	COMPLETE HANDOUTS	An Overview Of Microcomputer Systems (Cont'd)
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LEGION: An Experiment in Artificial Intelligence

By Marlin Ellers

Most articles about artificial intelligence start out with an introduction to the subject, a definition of artificial intelligence, and an apology to the many people in the field who disagree with the definition which the author has just put forth. One of the main reasons for this is that although most people agree upon the meaning of the word "artificial" very few agree upon the meaning of "intelligence", particularly when the critter that is claiming to have it is a machine. In an attempt to avoid quarrelsome definitions and hair-splitting arguments, and also in order to keep this article from becoming tediously long, your author will simply ignore the question of what artificial intelligence is for the time being and describe LEGION and allow the reader to come to his own conclusions and definitions.

THE PROBLEM

We would like to build a program that is capable of recognizing characters which are drawn as a dot matrix (see Fig. 1). Furthermore we would like the program to be able to "learn" what a character is by showing it several examples of a character and telling it what kind of character it is.

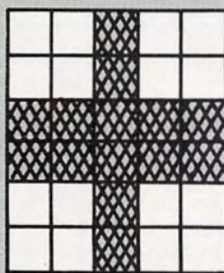


Figure 1. a 5x6 Dot Matrix Character (a plus sign)

LEGION

LEGION is the name of the program that the author wrote in a mixture of FORTRAN and Assembly Language in a couple of days that was an attempt to solve the above problem. It was not altogether successful, but it did have many interesting features and was quite fun to play with. Since LEGION was written quickly and sort of kluged together a general description is given rather than a listing.

The basic design decision was that LEGION would be made up of a number of small parts, each of which

was capable of deciding what it thought a character was, and each of which could be punished or rewarded for coming to a right or wrong decision.

The idea was that the parts that arrived at correct decisions most often would have a stronger say in the total decision that LEGION would finally make when asked about a character and thus with a little practice LEGION could learn what a character was. At this point it was decided that the parts would be called "citizen" and when LEGION was shown a character each "citizen" would "VOTE" on what kind of character he thought it was, and LEGION would simply tally the votes and see who the winner was. In addition each citizen would have a "bank account" which was essentially a tally of how often the "citizen" was right. Each time that a "citizen" guessed correctly a dollar was credited to his account. If, on the other hand he was wrong in his guess, he would lose a dollar from his account. When election time came to the community LEGION followed the very democratic principle of "one dollar," "one vote" thus weighting the "good" voters more heavily than the "bad" ones.

When LEGION was finally implemented several previously unspecified parameters of the problem were chosen in such a way as to simplify the programming on a 16-bit word machine, and to simplify the problem of inputting characters. (Recall that being a learning machine requires that a given character may have to be shown to the program several times before it will learn it. This does not present any problem to a system that has a card reader, but when all that you have

is a teletype and each character must be typed and retyped into the machine there is a definite need to keep the total input needed to a minimum).

For example, it was decided that a character would consist of a 5 by 6 diode matrix so that one character would fit conveniently into two 16-bit words (with two bits to spare). Also it was decided that LEGION would only be required to decide between four characters: a plus, a minus, a slash, and a zero.

A "citizen" voted on a particular character in this manner: a subroutine "VOTE" was called which treated a citizen (which consisted of a 16-bit number called his social security number or I.D. number) as a set of 16 switches that told whether to perform or not to perform certain fixed manipulations of the two words of character. For example, the first bit of the I.D. number tells whether or not to rotate the two words of character by one bit, the second tells whether or not to "Exclusive Or" the I.D. number in with the character etc. These manipulations were chosen at random in an attempt to insure that different "citizens" would scramble up the character quite differently. When a "citizen" was done scrambling the character it simply threw out all but the last two bits which it took as a number from one to four and that was that "citizen's" guess for that character. **Note** that this method means that an individual "citizen" is totally incapable of learning anything, for given the same character over and over again he will always scramble it the same way and will thus always make the same guess as to what it is.

LEGION is an interesting example of a whole that is equal to more than the sum of its parts, where a so-

ciety of inflexible unlearning individuals can work together to form a flexible learning body, just like a group of politicians (or worse yet, just the opposite).

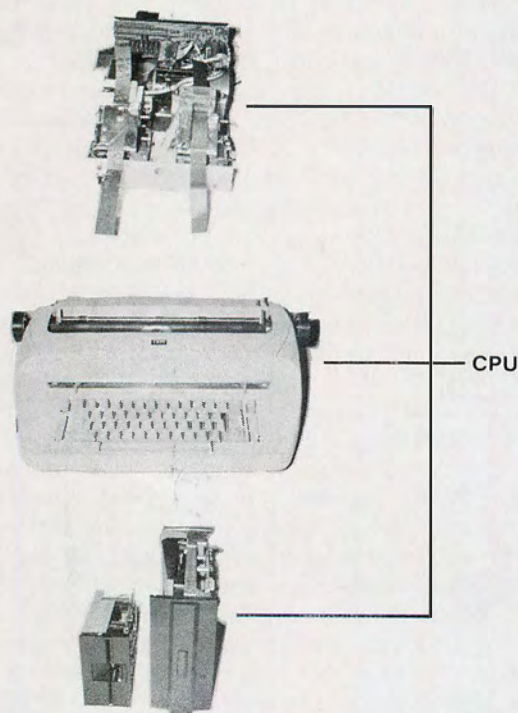
It was decided the LEGION would start out as a colony of 1000 people each with an initial bank account of \$15.00. Also since any "citizen" had a one out of four chance of guessing right on any one character it was decided that everyone would lose \$1.00 for a bad guess and gain \$3.00 for a correct guess thus keeping the total worth of the society at a steady level. Finally, in order to introduce new blood into society, it was decided that anyone that lost all of his money was clearly not worthwhile and would be replaced with a new individual who would start out with a fresh "bank account" of \$15.00. (The inflation introduced by this arbitrary introduction of new money was simply ignored. After all, normal people are forced to live with it so why should LEGION have it any better?) It took about three days to write and debug LEGION and he was ready for the big test, could he learn ???

THE TEST

LEGION was first shown the 20 characters shown in Fig. 2 and asked to sort them into the four previously described classes. He did not do an overly impressive job, getting 90% wrong the first time through. The teacher (the author) decided to see if LEGION could learn a single character. After showing a Plus about 10 times LEGION finally decided that the picture was a Plus instead of a zero. (Yea! a Victory). He was then shown another Plus. After about 4 showings LEGION decided that the second character was a Plus

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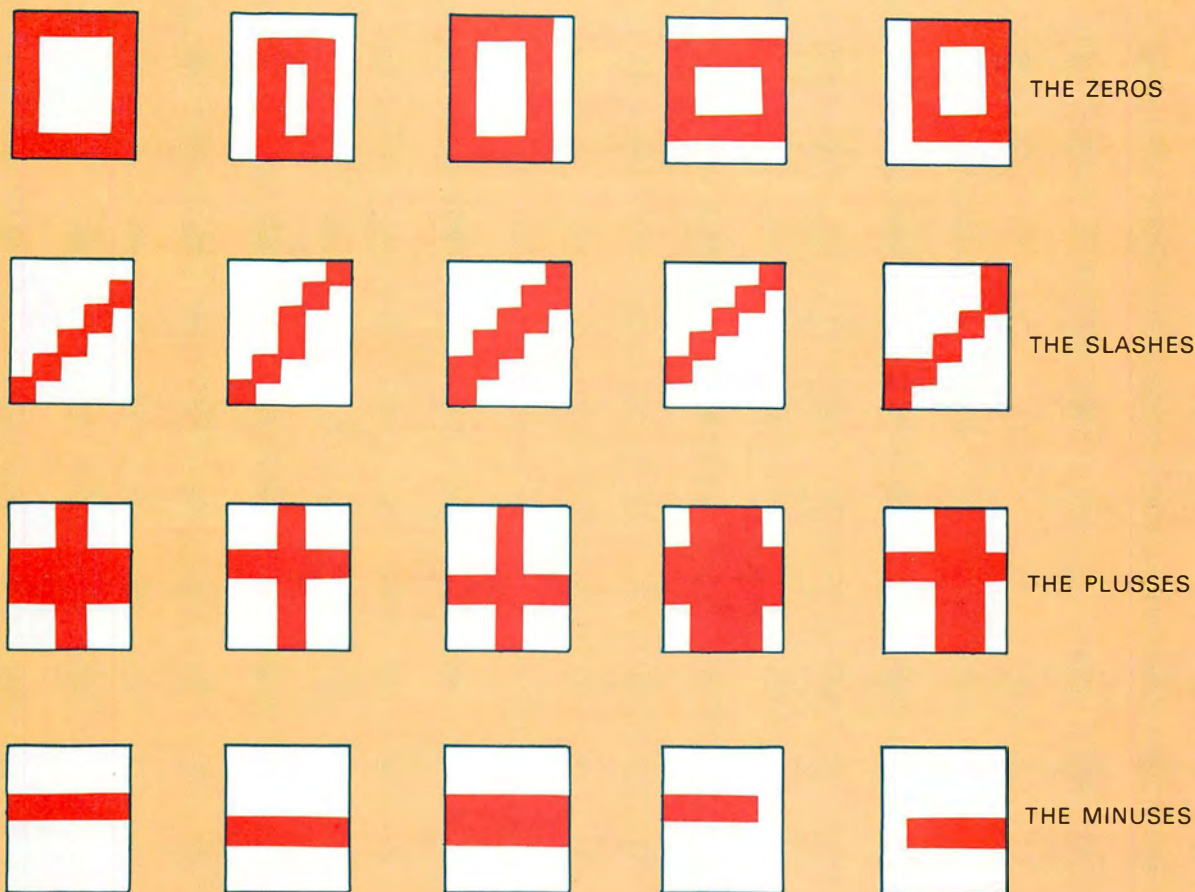


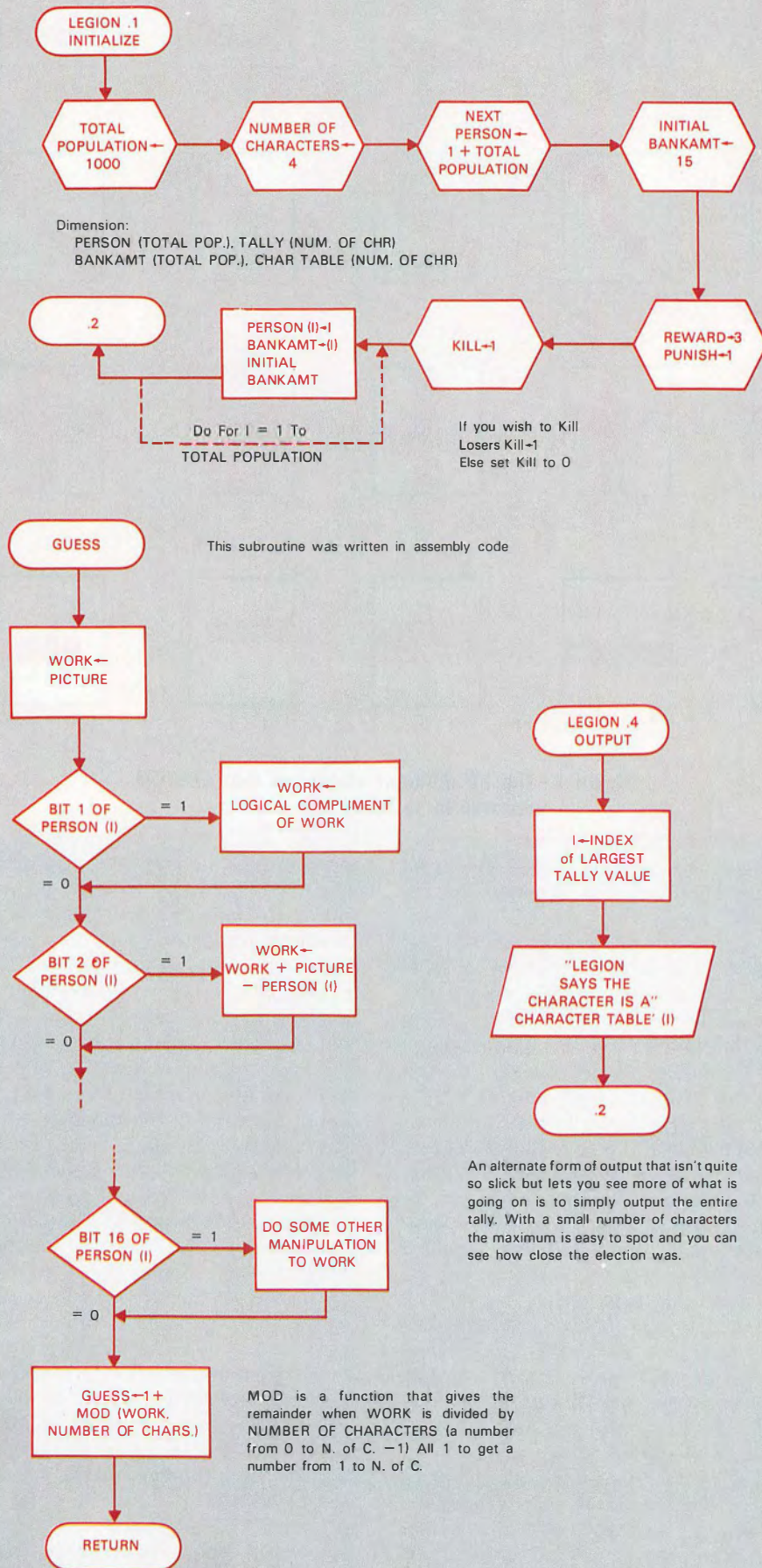
Figure 2. The 20 different characters that LEGION was trained to recognize.

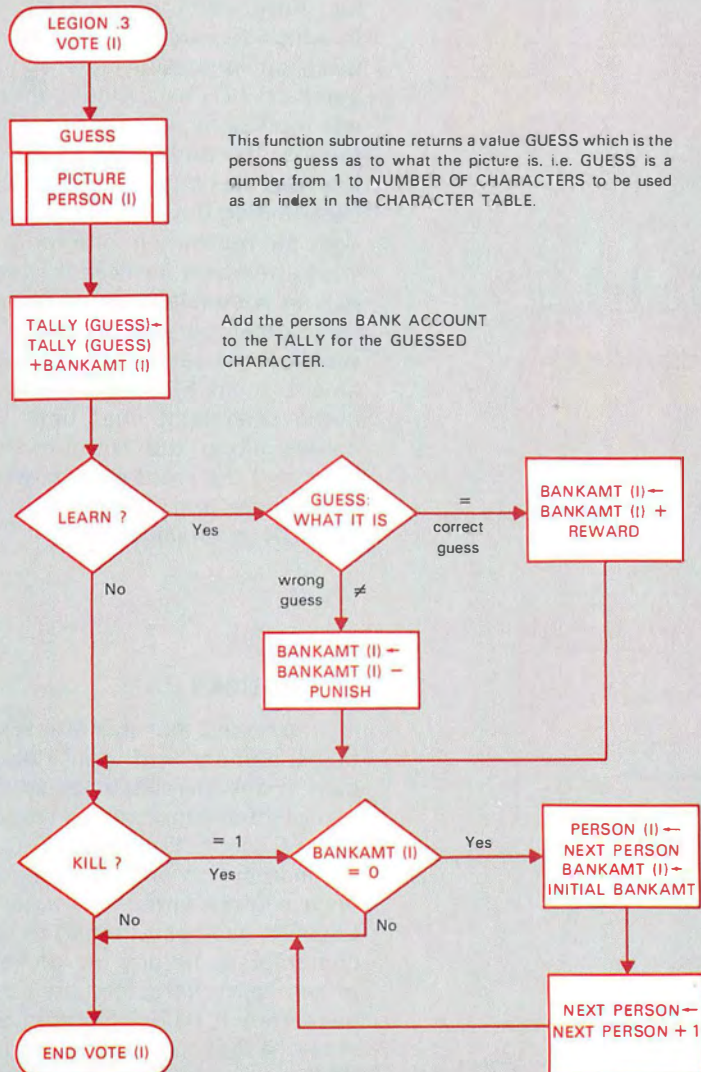
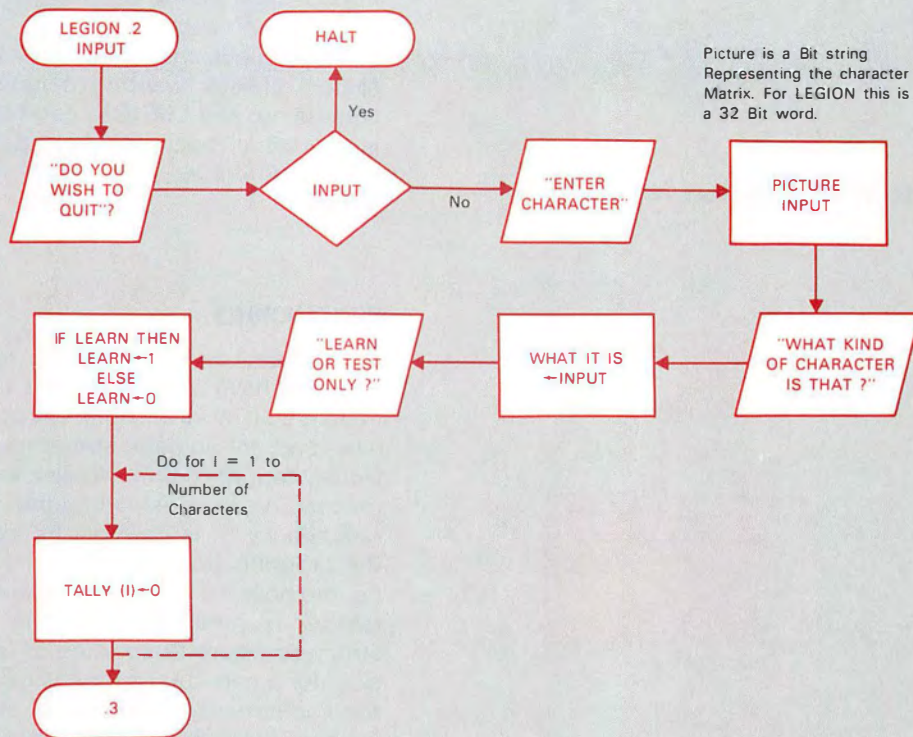
instead of a zero. (Yea! Another Victory). It was then reshown the first character, he guessed a zero (Tsk tsk you should remember longer than that). With one reshown however LEGION remembered that the first one was a Plus (Yea! again). After a little drill LEGION learned the Minus, and in the process forgot the Pluses. By alternating between the three of them LEGION eventually learned them all. After several hours of similar trials, familiar to every teacher LEGION had made considerable progress from an initial 90% wrong to 75% right. However in spite of this progress the teacher was frustrated that it was taking so long to learn what seemed to be such a simple task. The decision was that the teacher was simply being too lenient, "spare the rod and all that." Too many individuals that were not really any good were staying alive. After all, one could stay alive with guessing no better than random. Well that was quickly cured. With a fairly simple program change the penalty for failure to guess correctly was upped to \$2.00. The change that this brought over LEGION was simply amazing. Suddenly LEGION began to pick things up a little quicker and in short order was up to a perfect score, all 20 characters correctly identified.

At this point LEGION's brains were dismantled via a core dump in order to do some statistical checking and some curiosity satisfying; such as who had the biggest bank account? Was there a "perfect citizen," i.e. one who just happened to always be right? How many citizens were mediocre as compared to the rich ones,

i.e. were the rich an elite few who controlled most of society, or did the masses do most of the decision making? The surprising thing was that due to a programming bug there were citizens who had negative bank accounts! This was because under the old punishment system of up \$3.00 down \$1.00 it was decided to throw out someone when his bank account hit zero, so a test for zero was made. However under the new up \$3.00 down \$2.00 it was possible to have one's bank account go from +\$1.00 to -\$1.00 in one jump and thus get around the test for zero. This may have been partly responsible for the increased learning ability after the change, after all a citizen that consistently guesses wrong is just as valuable as one that is consistently right. The original classification as to "good" and "bad" citizens was wrong and unfair. A derelict who squanders his money performs valuable service to his society, and is cherished by the Creator (the author) as much as the model citizen who frugally tries to vote correctly in every election! Quite a revelation that may have far reaching consequences when applied to a society of actual persons. The old order was overthrown, a new paradigm came into being, a new method of introducing new blood had to be introduced. Was random death the answer? Is that the reason that all people must die? As he stood at that moment LEGION handled everything that had been thrown at him. Could he handle more? There was much interest in progressing further to see just what LEGION's limits were however at this point the powers

Figure 3. Detail Flowchart for LEGION

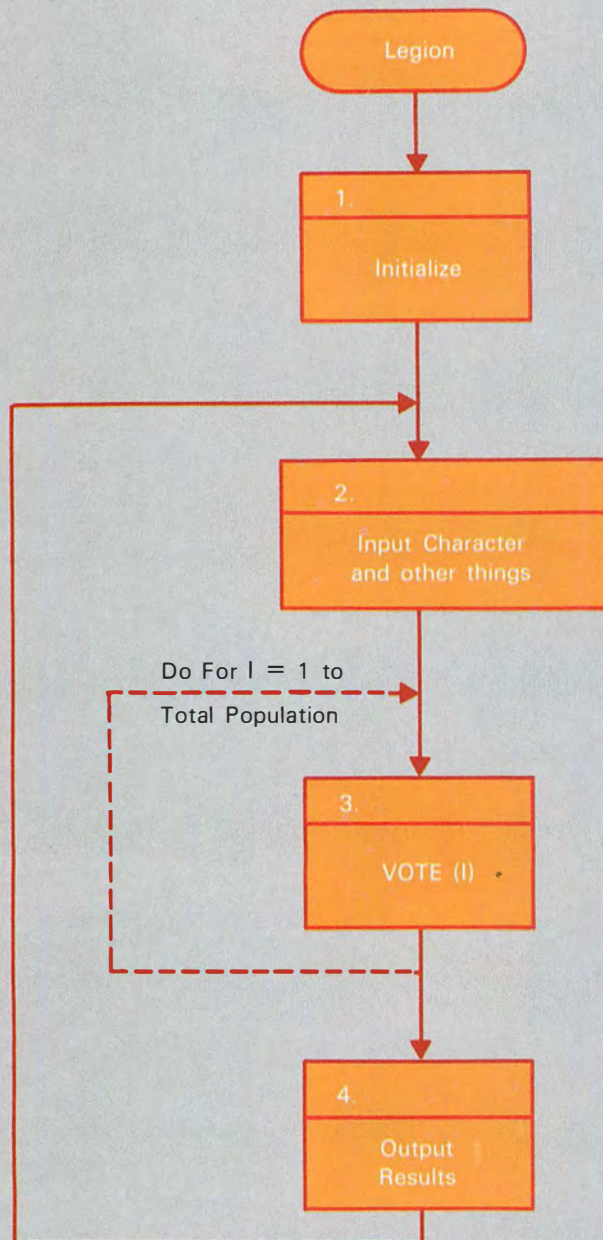




that be stepped in and asked what was going on and LEGION just barely jumped out the window in time to avoid being caught.

It has since that time, been a busy year, with customers always wanting a new operating system or something, and LEGION, good friend and kluge that he is, has never been resurrected, never been pushed to his full potential.

Figure 4. Overall Flowchart for LEGION



CONCLUSIONS

The question still remains, "Is LEGION intelligent?" He does have several on the tell-tale signs. For one thing LEGION is flexible enough to learn something new and to unlearn something that has been previously taught to him. He also exhibits a feature that is uncommon in most computer programs and that is redundancy. It is possible to erase great quantities of the program (the citizenry) and although he will lose his memory he is able to relearn everything. This last feature is reminiscent of the experiments in brain structure where the portion of the brain that is responsible for a particular action is isolated and removed but the impairment of function is only temporary, indicating that the brain has built in a certain redundancy of function. But is LEGION really intelligent? He can't tie his shoes, can't write poetry, can't even weave a web in which to catch flies for dinner and would surely receive an impossibly low score in the Stanford-Binet standard I.Q. test. Under those standards LEGION is not intelligent; but then neither are some of my best friends. The problem is in the definition of intelligence, it always has been. One test that has been put forth for determining if a machine possesses intelligence is that with the machine in one room and a person in another with a teletype for communication between them, the person is unable to tell if he is talking to a machine or to another person. LEGION would fail this test as would most readers if the person testing were only able to speak Mandarin Chinese. For these reasons the author maintains that until an acceptable definition comes along the Humpty-Dumpty criterion will be used and the word means what I want it to mean, nothing more and nothing less and under my definition LEGION is intelligent.

SUGGESTIONS

It is hoped that this article will inspire some readers to experiment with such learning programs on their own. If anyone should do so they may wish to try this test of intelligence which was going to be the next one for LEGION before he was so rudely interrupted. Does the learning on one character set enhance the learning on a slightly larger character set? In particular after LEGION has been trained to recognize the first twenty characters is he any more likely to be correct on a set of ten test characters than he would be if they had been shown before learning anything? Does he apply what he has previously learned to a new problem? Perhaps one of you can answer that.



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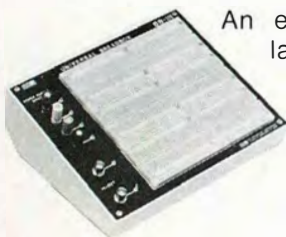
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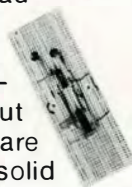
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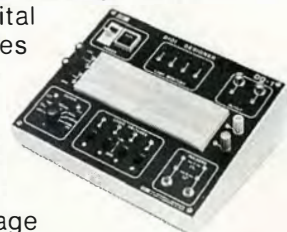
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FOREWORD

This stock option program is written in Processor Tech's 5K BASIC for the 8080 Microcomputer and requires 4.2K bytes of memory storage space.

INTRODUCTION

If you have an interest in the stock market or in listed call options, here's a way to use that interest to help pay for your home-brew system, buy some extra memory, or answer the inevitable question — "What *are* you going to do with your own computer?" The program described in this article calculates the net profit and rate of return for a simultaneous purchase of stock and sale of a call option, known generally as a *hedge* and specifically as covered writing.

WHAT IS AN OPTION?

A call option, or *call*, is the right to buy a number of shares of an underlying stock at a fixed price, called the strike or exercise price, until a fixed date, called the expiration date. Until recently, a buyer of *calls* had to go to a *call* broker who would find someone willing to offer (or write) a *call* at or near the price desired by the buyer. This method of buying and writing *calls* was relatively slow, and once a *call* was purchased, resale was difficult because there was no ready market for them.

In April, 1973, the Chicago Board Options Exchange (CBOE) began auction trading of *calls*, and a whole new world of investment strategies began with it. The CBOE's approach was simple. Each *call* would be in units of 100 shares, the strike price would be in increments of 5, 10, or 20 dollars per share (depending on the price of the underlying stock) and the expiration date would be fixed at one of four months of the year — January, April, July, and October. However, only three expiration periods would be traded at any one time. In addition, a liquid after-market would be maintained through a system of competing market makers. This meant that a *call* could be bought and sold minutes, hours, days, or weeks later depending on the buyer's assessment of market conditions. This idea was so successful that trading in *call* options grew from ten underlying stocks on the CBOE to nearly 200 underlying stocks on the CBOE, American Stock Exchange (AMEX), the Philadelphia, Baltimore and Washington (PHLX), the Pacific Coast Exchange (PCE), and Midwest Stock Exchange (MSE).

HOW OPTIONS WORK

To understand why CBOE type *calls* are so successful, the motives of buyer and writer alike need to be examined. First, we need a brief explanation of the interaction of stock and option prices. Using the stock prices of a hypothetical company, the cost of a *call* with a \$50 strike price at various stock prices with 6 months to go, 3 months to go, and at expiration is shown in Table 1.

MICROCOMPUTER STOCK OPTIONS

TO *HEDGE* OR NOT TO *HEDGE* —
THE OPTION IS YOURS



Until recently a buyer of *calls* had to go to a *call* broker. This method was relatively slow and resale was difficult.

By Edward Christianson

Table 1 — Cost of \$50 Strike Call Option

Stock Price	6 Months to go	3 Months to go	At Expiration
40	\$ 50	\$ 37	\$ 0
45	200	150	0
50	500	350	0
55	800	650	500
60	1,100	1,050	1,000
65	1,500	1,500	1,500

For example, if the stock was at \$45 per share, a 6 month *call* would cost \$200. If the stock was at \$55 per share, that same *call* would cost \$800.

The cost of a *call* can be divided into two parts:

1. **Premium** which represents the value for the time left until expiration. It decreases slowly in the first 5 to 6 months, then decreases much more rapidly during the last 3 months of life. For example, using the \$50 stock price in Table 1, a *call* may be worth \$500 with 6 months to go, \$350 with 3 months, and be worthless at expiration. Figure 1 shows a relationship between *premium* and time.

There are other factors which influence *premiums*. The options of more volatile stocks, which move up quickly during rallies, command higher *premiums*. The supply and demand for options on the floor of the exchange also influences the *premium*. Also, a significant dividend from an "income" stock represents added income to the writer. *Call* buyers recognize this income, and adjust their bids on *calls* accordingly.

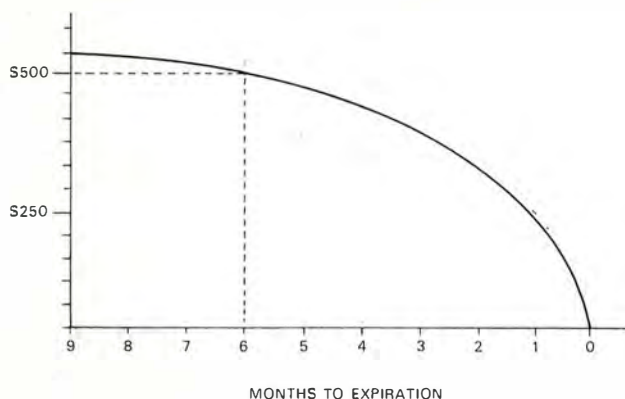


Figure 1. Premium vs Time

2. **Intrinsic value** is the stock price minus the strike price and is always positive. The relationship of intrinsic value in the cost of a call can best be explained in Figure 2. For example, notice that when the stock price is \$55, the option cost is \$800. The *intrinsic value* is \$500 and the *premium* is \$300.

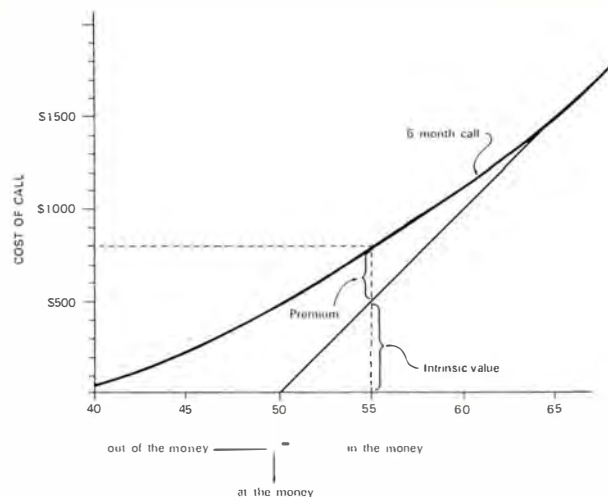


Figure 2. \$50 Strike Call — Prices vs Stock Price

Several items should be noted here. First, as the stock price increases, the *intrinsic value* increases, dollar for dollar, *once* the stock price has risen above the strike price. *Secondly*, the *premium* virtually disappears when the stock price is 25% to 30% above its strike price.

When the stock price is above the strike price, the *call* is said to be "in the money." When the stock price is below the strike, the *call* is "out of the money." When the stock price is equal or nearly equal to the strike, the *call* is "at the money."

Using the prices from Table 1, we will calculate the profits, the capital requirements, and the return on investment for a buyer, a naked writer, and a covered writer. A naked writer is one who writes (offers) the option, but does not own the underlying stock. A covered writer owns the stock when the call is originally written.

THE OPTION BUYER

In this example, assume the stock is at \$50 per share, and a 6 month \$50 *call* is purchased for \$500. Brokerage fees, dividends, and margin interest costs are ignored.

Stock Price	Value of Call	Profit (Loss)	Capital Required	Return %
40	\$ 0	\$-500	\$500	-100
45	0	-500	500	-100
50	0	-500	500	-100
55	500	0	500	0
60	1,000	500	500	100
65	1,500	1,000	500	200

Table 2 — Profit or Loss at Expiration — Buyer

In a sharply rising market, buying *calls* is an excellent strategy.

The buyer risks 100% of his capital. In fact, the stock must rise 10% (from 50 to 55) before he breaks even. After that, however, the rewards are quite dramatic. A 20% rise (from 50 to 60) will not only cover his costs, but will result in a 100% profit. In a sharply rising market, buying *calls* is an excellent strategy.

... Not for the beginner in options.

THE NAKED WRITER

In this example, the stock is at \$50 per share, and a \$50 strike *call* is written with \$500 in proceeds to the writer. Again, brokerage, dividends, and margin interest are ignored.

A naked writer is required to put up at least 30% of the cost of delivering the shares. In addition, when the stock price is above the strike price, he must put up additional capital, dollar for dollar for each share for which he is naked. For example, when the stock is \$5 above the strike, he would be required to put up another \$500 in capital. On the other hand, if the stock was below the strike price, his capital requirements would be lowered, again dollar for dollar for each share. If the stock was \$5 below the strike, the capital required would be lowered by \$500. This process is called *marking* to the market.

Stock Price	Value of Call	Profit (Loss)	Capital Required	Return %
40	\$ 0	\$ 500	500	100
45	0	500	1,000	50
50	0	500	1,500	33
55	500	0	2,000	0
60	1,000	-500	2,500	-20
65	1,500	-1,000	3,000	-33

Table 3 — Profit or Loss at Expiration — Naked Writer

The naked writer has an excellent return in a declining market. On the other hand, the capital requirements increase very rapidly because of the *marking* to the market requirements. A sudden, sharp rally could cause the naked writer to run out of capital. At this point, the brokerage firm would close out his position, resulting in a severe loss to the writer.

THE COVERED WRITER

In this example, the writer sets up his position by simultaneously buying the stock (100 shares at \$50 per share) and offering the 6 month option, receiving \$500 as proceeds. In any *hedge* transaction, the capital required is offset by the proceeds of the sale. Thus, the net capital required is \$4,500 (5000—500). At or near expiration, two alternatives are possible.

Alternative 1. Allow the *call* to be exercised and deliver

the stock. If the *call* is not exercised, the stock may be sold or another *call* may be offered against it. For purposes of this example, assume the stock is delivered or sold.

Stock Price	OPTION		STOCK		Capital Required	Return %
	Value of Call	Profit (Loss)	Value	Profit (Loss)		
40	\$ 0	\$500	\$4,000	\$-1,000	\$4,500	-11
45	0	500	4,500	-500	4,500	0
50	0	500	5,000	0	4,500	11
55	a	500	b	0	4,500	11
60	a	500	b	0	4,500	11
65	a	500	b	0	4,500	11

Table 4 — Profit or Loss at Expiration — Covered Writer

Result a. To the writer, the value of the *call* if it is exercised is irrelevant — he has made his \$500 profit.

Result b. Since he delivers the stock at \$50 per share, his proceeds will be \$5,000, regardless of the current market price of the stock.

Alternative 2. Close out the position before expiration by buying back the option and selling the stock.

Stock Price	OPTION		STOCK		Capital Required	Return %
	Value of Call	Profit (Loss)	Value	Profit (Loss)		
40	\$ 0	\$ 500	\$4,000	\$-1,000	\$-500	-11
45	0	500	4,500	500	0	0
50	0	500	5,000	0	500	11
55	500	0	5,500	500	500	11
60	1,000	-500	6,000	1,000	500	11
65	1,500	-1,000	6,500	1,500	500	11

Table 5 — Profit or Loss from Early Closeout — Covered Writer

The net results are the same but there are reasons for choosing the second alternative over the first as we shall see later.

The covered writer limits his profit somewhat, but in return, he has more protection against loss. Covered writing strategies work best in flat or rising markets.

LEVERAGE

Leverage is using a small amount of capital to control a larger amount of capital. For example, a \$500 *call* controls \$5,000 worth of stock, a *leverage* ratio of 10 to 1. Though covered writing is the most conservative of the three methods, through increased *leverage*, the return can be substantially increased. The covered writer uses a margin account which allows him to borrow capital (current 50%) to set up a position. In

return, the brokerage firm charges interest, called *margin* interest, on the capital borrowed, usually at not less than 1/2% above the prime rate.

THE COVERED WRITER—MARGINED

Next, we shall re-examine the same covered writing *hedge* using *margin*, again excluding brokerage fees, dividends, and *margin* interest. The capital required is 50% of the stock purchase minus the proceeds from the sale of the option. Assume the position is closed out as in Alternative 2.

Stock Price	Value of Call	Profit (Loss)	Value	Profit (Loss)	Profit (Loss)	Capital Required	Return %
40	\$ 0	\$ 500	\$4,000	\$-1,000	\$ -500	\$2,000	-25
45	0	500	4,500	-500	0	2,000	0
50	0	500	5,000	0	500	2,000	25
55	500	0	5,500	500	500	2,000	25
60	1,000	-500	6,000	1,000	500	2,000	25
65	1,500	-1,000	6,500	1,500	500	2,000	25

**Table 6 — Profit or Loss
from Early Closeout —
Margined Covered Writer**

Note that the return is now 25% instead of 11%. However, the percentage loss possible is also increased.

Choose a broker who specializes in options, who understands *hedges* ... and recommends suitable strategies in tune with your money.

BROKERAGE FEES

During the previous examples, we have ignored brokerage fees, dividends and *margin* interest. However, in the real world, they represent 30% or more of the total profit. Since May, 1975, brokers' fees have been negotiable, with the better customers getting larger discounts from the old rate structure. A recent development is the rise of the "discount" brokerage firm. Fully regulated, they do not offer market research nor recommendations, but merely execute your orders on the stock exchanges at discounts of 30% or more from the previous rate structure. In addition, many stocks, some of which have listed *call* options, are traded directly between brokerage firms as well as the floor of the major exchanges. Direct trading in this manner is known as over the counter (OTC) or the third market. Commissions are less on the OTC than on the major exchanges.

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THE PROGRAM OUTPUT

The best way to demonstrate the effect of brokerage fees is to run our *margined* covered writer example through the program. The output is divided into four sections — Heading, Cost, Proceeds, and Return.

The Heading section gives the date of the evaluation, and restates the *hedge* — number of shares bought and number of options sold.

The Cost section includes the cost of the shares, the brokerage fees to buy the shares (labeled IN), to deliver the shares (labeled OUT), and to sell the option (labeled OPTION), and the *margin* interest cost. The Proceeds section includes the money received from delivering the shares at the strike price, the money from the sale of the options, and dividends (if any).

The Return section includes the net profit (total proceeds minus total cost), the net capital required, the percent net return, the number of days to expiration, the annual rate of return and the breakeven point. The breakeven point is the price of the stock (at expiration) where no profit will be made. It is computed by subtracting net profit from the original purchase cost.

Figure 3 is sample output of our *margined* covered writer using the New York Stock Exchange brokerage rates, and Figure 4 uses the OTC rates.

```

READY
RUN

INPUT MM,DD,YY, MARGIN? (1=YES), LOAN RATE (#.##)

?12,16,76,1,7.50
OUTPUT TO BE 32 OR 64 CHARACTERS?
?64
EVALUATION NO, DIVIDEND ($/SHARE/QTR)

?1,10
NO. SHARES, PRICE/SHARE, MARKET (1=NYSE, 2=OTC)

?100,50,1
EXPIRATION MONTH, STRIKE, COST/OPTION

?6,50,500

COVERED WRITE NO 1 12 16 76
BUY 100 SHARES AT 50
SELL 1 6 50 'S AT $ 500 EACH

      COST          PROCEEDS          RETURN
YOUR $ 2500        STOCK 5000        $ 312.00
LOAN $ 2500        OPTION 500        2188 IS
BROKER'S          DIVIDEND 20        14.2 %
      IN 51
      OUT 51
      OPTION 26
      MARGIN 80
      -----
TOTALS 5208        -----
MORE? (1=YES)      5520        $ 46.8
?1
  
```

Figure 3. Sample Using NYSE Brokerage Rate

In any *hedge* transaction, the capital required is offset by the proceeds of the sale.

```

EVALUATION NO, DIVIDEND ($/SHARE/QTR)

?2,10
NO. SHARES, PRICE/SHARE, MARKET (1=NYSE, 2=OTC)

?100,50,2
EXPIRATION MONTH, STRIKE, COST/OPTION

?6,50,500

COVERED WRITE NO 2 12 16 76
BUY 100 SHARES AT 50
SELL 1 6 50 'S AT $ 500 EACH

      COST          PROCEEDS          RETURN
YOUR $ 2500        STOCK 5000        $ 366.00
LOAN $ 2500        OPTION 500        2134 IS
BROKER'S          DIVIDEND 20        17.1 %
      IN 25
      OUT 25
      OPTION 26
      MARGIN 78
      -----
TOTALS 5154        -----
MORE? (1=YES)      5520        $ 46.3
?0
  
```

STOP IN LINE 145

READY

Figure 4. Sample Using OTC Brokerage Rate

The annual rate of return will be increased if the months until the premium is gone can be shortened.

COMPOUNDING YOUR PROFITS

Another way to increase *leverage* is by compounding your profits. In the case of the covered writer, compounding is accomplished by taking the profit as soon as it becomes available and immediately re-investing it, rather than waiting until expiration. The effect of compounding can best be demonstrated through a measure called the annual rate of return which is calculated as follows:

$$\text{ANNUAL RATE OF RETURN} = \frac{\text{rate of return \%}}{\text{months until premium is gone}} \times \frac{12 \text{ months}}{\text{months until premium is gone}}$$

In our previous example, the

$$\text{ANNUAL RATE OF RETURN} = 25\% \times 12/6 = 50\%$$

The annual rate of return will be increased if the months until the *premium* is gone can be shortened. Referring again to Table 1 or Figure 2, notice that the *premium* disappears when the stock price rises high enough. Suppose our *margined* covered writer notices 3 months later that the stock is now at \$65, and the option cost is \$1,500. He can close out his position now, and pocket the \$500 profit. Look what happens to the annual rate of return.

$$\text{ANNUAL RATE OF RETURN} = 25\% \times 12/3 = 100\%$$

He is now free to evaluate market conditions and enter into a new *hedge*.

RUNNING THE PROGRAM

You will need the latest option quotations. Either the Wall Street Journal (daily) or Barron's Weekly is a complete, and reliable source. The program requires input in the following order:

Option	Sales (100s)	Open Int.	High	Low	Last	Chg.	Net Stock Close
N C R	Jan25.....	4	315	11	10 5/8	11 + 1 1/2	36 1/4
N C R	Jan30.....	290	1398	6 1/4	4 7/8	6 1/4 + 1	36 1/4
N C R	Jan35.....	1073	5905	2	1 3/8	1 13-16 + 7-16	36 1/4
N C R	Apr30.....	51	434	7 1/4	6	7 1/4 + 1	36 1/4
N C R	Apr35.....	751	2598	3 3/8	2 9-16	3 3/8 + 7-16	36 1/4
N C R	Jul30.....	14	88	7 3/8	6 3/4	7 1/4 + 1/4	36 1/4
N C R	Jul35.....	226	778	4 1/4	3 1/2	4 + 3/8	36 1/4
N Semi	Feb25.....	2867	3892	5 1/8	4	4 1/4.....	27 7/8
N Semi	Feb30.....	5872	11712	2 1/8	1 9-16	1 11-16 - 1-16	27 7/8
N Semi	Feb35.....	3182	12388	3/4	1/2	1/2 - 1-16	27 7/8
N Semi	Feb40.....	578	8502	3-16	1/8	1/8 - 1-16	27 7/8
N Semi	Feb45.....	228	4854	1/8	1-16	1-16.....	27 7/8
N Semi	Feb50.....	3	5094	1-16	1-16	1-16.....	27 7/8
N Semi	May25.....	788	2261	6 1/4	5 3/8	5 1/2 - 1/4	27 7/8
N Semi	May30.....	2287	6933	3 3/8	2 15-16	3 - 1/8	27 7/8
N Semi	May35.....	1800	6958	1 3/4	1 3/8	1 7-16 - 1/8	27 7/8
N Semi	May40.....	1457	5188	13-16	9-16	11-16.....	27 7/8
N Semi	Aug25.....	588	853	7 1/4	6 1/4	6 3/8 - 1/8	27 7/8
N Semi	Aug30.....	1233	1712	4 1/2	3 3/4	3 7/8 - 1/8	27 7/8
Nw Air	Jan25.....	56	411	5 3/8	5	5 1/4 - 1/8	29 3/4
Nw Air	Jan30.....	551	3027	1 3/8	1 3-16	1 3-16 - 3-16	29 3/4
Nw Air	Jan35.....	225	2280	5-16	1/8	1/8 - 1/8	29 3/4
Nw Air	Apr25.....	33	143	6	5 3/8	5 7/8 + 1/8	29 3/4
Nw Air	Apr30.....	250	1662	2 11-16	2 3/8	2 3/8 - 1/8	29 3/4
Nw Air	Apr35.....	167	1377	15-16	3/4	13-16 - 1-16	29 3/4
Nw Air	Jul25.....	4	131	6 3/4	6 3/4	6 3/4 - 1/4	29 3/4
Nw Air	Jul30.....	131	606	3 1/2	3	3 - 1/8	29 3/4
Occi	Feb15.....	1359	2410	7 1/4	5 3/4	6 7/8 + 3/8	21 7/8
Occi	Feb20.....	7458	21020	2 7-16	1 9-16	2 1-16 + 1/4	21 7/8
Occi	May15.....	622	2146	7 3/8	6 1/8	7 + 3/8	21 7/8
Occi	May20.....	2807	10179	3 1/4	2 3-16	2 7/8 + 7-16	21 7/8
Occi	Aug15.....	330	437	7 1/2	6 1/4	7 1/4 + 1/2	21 7/8
Occi	Aug20.....	1329	2776	3 3/4	2 3/4	3 3/8 + 7-16	21 7/8
Pennz	Jan25.....	57	416	7 1/2	7	7 1/4 - 1/4	32 1/8
Pennz	Jan30.....	458	2815	2 7/8	2 1/8	2 7-16 - 1-16	32 1/8
Pennz	Jan35.....	290	3667	3/8	3-16	3-16 - 3-16	32 1/8
Pennz	Apr25.....	37	44	7 3/8	7 1/8	7 1/2 - 1/8	32 1/8
Pennz	Apr30.....	358	1615	3 3/4	3	3 1/4.....	32 1/8
Pennz	Apr35.....	316	1939	1 3-16	7/8	1 - 1/8	32 1/8
Pennz	Jul25.....	24	82	7 3/4	7	7 3/4 + 1/4	32 1/8
Pennz	Jul30.....	56	533	4 1/4	3 7/8	3 7/8 - 1/8	32 1/8
Pepsi	Jan70.....	162	191	13 3/8	11 1/8	11 1/8 - 7/8	80 3/4
Pepsi	Jan80.....	246	548	4 1/4	2 1/4	2 1/2 - 3/4	80 3/4
Pepsi	Jan90.....	237	347	3/8	3-16	5-16.....	80 3/4
Pepsi	Apr70.....	63	86	14 1/2	13	13 3/8 + 1 1/4	80 3/4
Pepsi	Apr80.....	111	267	6	4 1/2	4 5/8 - 1/4	80 3/4
Pepsi	Apr90.....	34	400	2	1 3/8	1 3/8.....	80 3/4
Pepsi	Jul80.....	19	66	7 1/4	5 3/4	5 3/4 - 1/2	80 3/4
Pepsi	Jul90.....	16	110	2 3/8	2 3/8	2 3/8.....	80 3/4
Polar	Jan30.....	2934	2907	10 3/4	7 1/2	8 3/4 + 1 3/8	38 7/8
Polar	Jan35.....	7460	8838	5 7/8	3 3/8	4 1/4 + 1	38 7/8
Polar	Jan40.....	16 81	23304	2 1-16	7/8	1 7-16 + 9-16	38 7/8
Polar	Apr35.....	2442	4858	7 1/8	5	5 5/8 + 7/8	38 7/8
Polar	Jul35.....	642	2421	8	6	6 3/4 + 3/4	38 7/8
Polar	Apr40.....	6543	10529	5 1/4	2 3/8	2 7/8 + 9-16	38 7/8
Polar	Jan45.....	2836	14935	9-16	3-16	7-16 + 5-16	38 7/8
Polar	Apr45.....	2988	6349	1 15-16	15-16	1 3/8 + 7-16	38 7/8
Polar	Jul40.....	1720	3445	5	3 3/8	4 + 3/4	38 7/8
R C A	Jan20.....	386	290	7 3/8	5 1/8	7 1/8 + 2	26 5/8
R C A	Jan25.....	3547	7624	2 3/8	1	2 1/8 + 1 1/8	26 5/8
R C A	Jan30.....	1375	12628	1/4	1-16	3-16 + 1-16	26 5/8
R C A	Apr20.....	103	193	7 3/8	5 3/8	7 1/4 + 1 7/8	26 5/8
R C A	Apr25.....	1803	5112	3 1/8	1 13-16	2 7/8 + 1 1/8	26 5/8
R C A	Apr30.....	1714	7316	15-16	7-16	13-16 + 5-16	26 5/8
R C A	Jul20.....	108	257	7 1/2	5 3/4	7 1/4 + 1 5/8	26 5/8
R C A	Jul25.....	623	2322	3 3/8	2 5-16	3 1/2 + 1 1/8	26 5/8
Raythn	Feb50.....	8	67	12	11 3/8	11 7/8 + 2 3/8	61 1/8
Raythn	Feb60.....	116	802	4 1/4	3 1/4	3 1/4 + 3/8	61 1/8
Raythn	Feb70.....	6	672	5-16	1/4	5-16 + 1-16	61 1/8
Raythn	May60.....	23	205	5 3/4	5	5 1/8 + 1	61 1/8
Raythn	May70.....	81	336	1 1/2	1 1-16	1 1/4 + 1/8	61 1/8
Raythn	Aug50.....	4.....	12 1/2	12 1/2	12 1/2.....	61 1/8	61 1/8
Raythn	Aug60.....	5	47	6 3/4	6 1/2	6 3/4 + 1 1/2	61 1/8

Example. Excerpt from Barron's Option Quotation

RUN

INPUT MM,DD,YY, MARGIN? (1=YES), LOAN RATE (#.##)

?12,10,76,1,7.5

OUTPUT TO BE 32 OR 64 CHARACTERS?

?64

EVALUATION NO, DIVIDEND (\$/SHARE/QTR)

?101,.08

NO. SHARES, PRICE/SHARE, MARKET (1=NYSE, 2=OTC)

?200,38.87,2

EXPIRATION MONTH, STRIKE, COST/OPTION

?4,35,562

COVERED WRITE NO 101 12 10 76

BUY 200 SHARES AT 38.87

SELL 2 4 35 'S AT \$ 562 EACH

	COST	PROCEEDS	RETURN
YOUR \$	3887	STOCK 7000	\$ 169.0N
LOAN \$	3887	OPTION 1124	2944 IS
BROKER'S		DIVIDEND 16	5.7 %
IN	42		131 DAYS
OUT	42		= 15.8 %
OPTION	36		ANNUALLY
MARGIN	77		BRK-EVEN
	-----	-----	IS
TOTALS	7971	8140	\$ 38
MORE? (1=YES)			
?1			

Example 1. Using Polaroid April 35's

EVALUATION NO, DIVIDEND (\$/SHARE/QTR)

?102,.08

NO. SHARES, PRICE/SHARE, MARKET (1=NYSE, 2=OTC)

?200,38.87,2

EXPIRATION MONTH, STRIKE, COST/OPTION

?4,40,287

COVERED WRITE NO 102 12 10 76

BUY 200 SHARES AT 38.87

SELL 2 4 40 'S AT \$ 287 EACH

	COST	PROCEEDS	RETURN
YOUR \$	3887	STOCK 8000	\$ 609.0N
LOAN \$	3887	OPTION 574	3504 IS
BROKER'S		DIVIDEND 16	17.3 %
IN	42		131 DAYS
OUT	42		= 48.2 %
OPTION	32		ANNUALLY
MARGIN	91		BRK-EVEN
	-----	-----	IS
TOTALS	7981	8590	\$ 35.8
MORE? (1=YES)			
?1			

Example 2. Using Polaroid April 40's

EVALUATION NO, DIVIDEND (\$/SHARE/QTR)

?103,.08

NO. SHARES, PRICE/SHARE, MARKET (1=NYSE, 2=OTC)

?200,38.87,2

EXPIRATION MONTH, STRIKE, COST/OPTION

?4,45,137

COVERED WRITE NO 103 12 10 76

BUY 200 SHARES AT 38.87

SELL 2 4 45 'S AT \$ 137 EACH

	COST	PROCEEDS	RETURN
YOUR \$	3887	STOCK 9000	\$ 1304.0N
LOAN \$	3887	OPTION 274	3809 IS
BROKER'S		DIVIDEND 16	34.2 %
IN	42		131 DAYS
OUT	42		= 95.2 %
OPTION	29		ANNUALLY
MARGIN	99		BRK-EVEN
	-----	-----	IS
TOTALS	7986	9290	\$ 32.3
MORE? (1=YES)			
?1			

Example 3. Using Polaroid April 45's

INPUT	SOURCE
MM.DD.YY	This is the month, day, and year of the quotations.
MARGIN? (1=YES)	If the stock is bought on <i>margin</i> , enter a 1, otherwise enter any number.
LOAN RATE (#.##)	This is the <i>margin</i> interest rate, expressed as a percentage. It is usually ½% above the prime lending rate. Ask your broker or use 7.50 as a good approximation.
OUTPUT TO BE 32 OR 64 CHARACTERS	The output is 16 lines high, and can be either 32 or 64 characters wide.
EVALUATION NO.	Your choice. If the program could handle strings, it would be the stock name.
DIVIDEND (\$/SHARE/QTR.)	This information is available from many sources, including Barron's. It can be zero.
NO. SHARES	The number of shares purchased. It must be in multiples of 100 shares.
PRICE/SHARE	Fractional prices must be converted to decimal prices, for example 37 ¼ is 37.25. This information will be the last item in each line of the option quotations.
MARKET (1=NYSE,2=OTC)	Ask your broker if the stock can be purchased in the 3rd (OTC) market.
EXPIRATION MONTH	This is the number of the expiration month, 1=January, 4=April, etc. The program assumes all options expire on the 20th day.
STRIKE	On your option quotations, this is the number next to the month. For example, a "Jan35" is an option which expires in January and has a strike of \$35/share.
COST/OPTION	Option prices are given on a per share basis. To compute the total cost per option, multiply the price by 100. For example, 2% is \$237.50 per option. Use the last or closing prices as input.

RUN

INPUT MM.DD.YY, MARGIN? (1=YES), LOAN RATE (0.##)

```
?12,10,76,1,7.5
OUTPUT TO BE 32 OR 64 CHARACTERS?
?32
EVALUATION NO, DIVIDEND ($/SHARE/QTR)
?104,.08
NO. SHARES, PRICE/ SHARE, MARKET (1=NYSE, 2=OTC)
?200,35,0
??0
EXCHANGE IS 1 OR 2 0
NO. SHARES, PRICE/ SHARE, MARKET (1=NYSE, 2=OTC)
?200,38.87,2
EXPIRATION MONTH, STRIKE, COST/OPTION
?1,35,425
COVERED WRITE NO 104 12 10 76
BUY 200 SHARES AT 38.87
SELL 2 1 35 'S AT $ 425 EACH
      COST      PROCEEDS      RETURN
YOUR $ 3887 STOCK 7000 $-68 ON
LOAN $ 3887 OPTION 850 3181 IS
BROKER'S DIVIDEND -2.1 %
      IN      42      41 DAYS
      OUT      42      =-18.6 %
      OPTION 34      ANNUALLY
MARGIN 26      BRK-EVEN
      ----- IS
TOTALS 7918      7850 $ 39.2
MORE? (1=YES)
?1
```

Example 4. Using Polaroid January 35's

EVALUATION NO, DIVIDEND (\$/SHARE/QTR)

?105,.08

NO. SHARES, PRICE/ SHARE, MARKET (1=NYSE, 2=OTC)

?200,38.87,2

EXPIRATION MONTH, STRIKE, COST/OPTION

?1,40,144

COVERED WRITE NO 105 12 10 76

BUY 200 SHARES AT 38.87

SELL 2 1 40 'S AT \$ 144 EACH

COST	PROCEEDS	RETURN
YOUR \$ 3887	STOCK 8000	\$ 369 ON
LOAN \$ 3887	OPTION 288	3744 IS
BROKER'S	DIVIDEND	9.8 %
IN 42		41 DAYS
OUT 42		= 87.2 %
OPTION 30		ANNUALLY
MARGIN 31		BRK-EVEN
-----	-----	IS
TOTALS 7919	8288	\$ 37

MORE? (1=YES)
?0

STOP IN LINE 145

Example 5. Using Polaroid January 40's

The editing of data is extensive. Any item which is used in the computation is checked for reasonableness. If multiple errors exist in an input line, each one is described briefly along with the erroneous value before the datum is to be reinput.

By studying the examples given with the actual data, it will be apparent that there is a considerable difference between the rate of return for various strike prices, even with the same expiration date. This difference depends on whether the option is in, at, or out of the money. The option you choose depends upon your investment goals, your assessment of the market in general, and your stock during the life of the option. Figure 5 below illustrates this relationship.

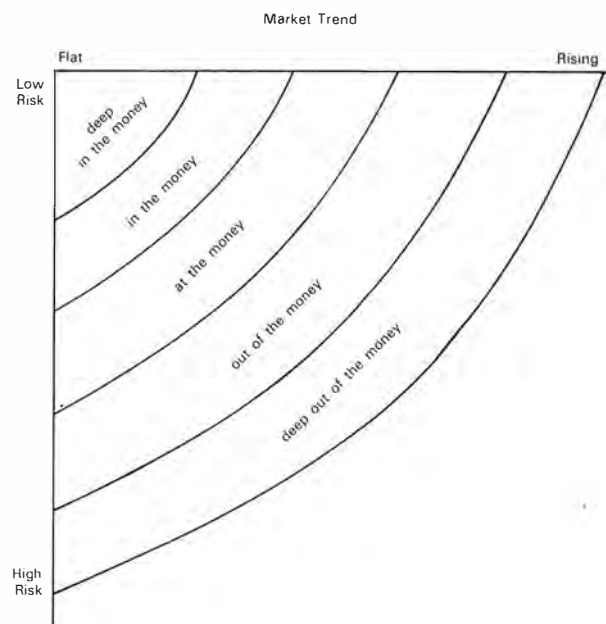


Figure 5. Market Trend vs Risk

When available a deep "in the money" *call* would be two or more strikes below the "at the money" *call*. A deep "out of the money" *call* would be two or more strikes above the "at the money" *call*.

GETTING STARTED

If you are ready for option writing, I recommend that you do some further reading. Three excellent books available on option strategies are listed at the end of this article. They also include sections on income tax requirements, a subject certainly worth studying. Choose a broker who specializes in options, who understands *hedges*, order placement, floor execution, and most importantly, your investment goals and will recommend suitable strategies in tune with these goals. Don't settle for less, remember it's your money!

A special thanks to Ward Christenson for the use of his ALTAIR 8800 system and assistance during one marathon session of inputting, debugging and testing.

PROGRAM SPECIFICATIONS AND REMARKS

The program is written in Processor Tech 5K Basic. Because of extensive comments and editing, its size is about 4.2K. Eliminating the comments and making the edit error descriptions more cryptic could reduce it to about 3K.

SUGGESTED READING

The New Options Market by Max G. Ansbacher (Walker & Co.). A good book for the beginning student of op-

tions. He covers strategies for buying options, naked writing, covered writing as well as more advanced strategies using options.

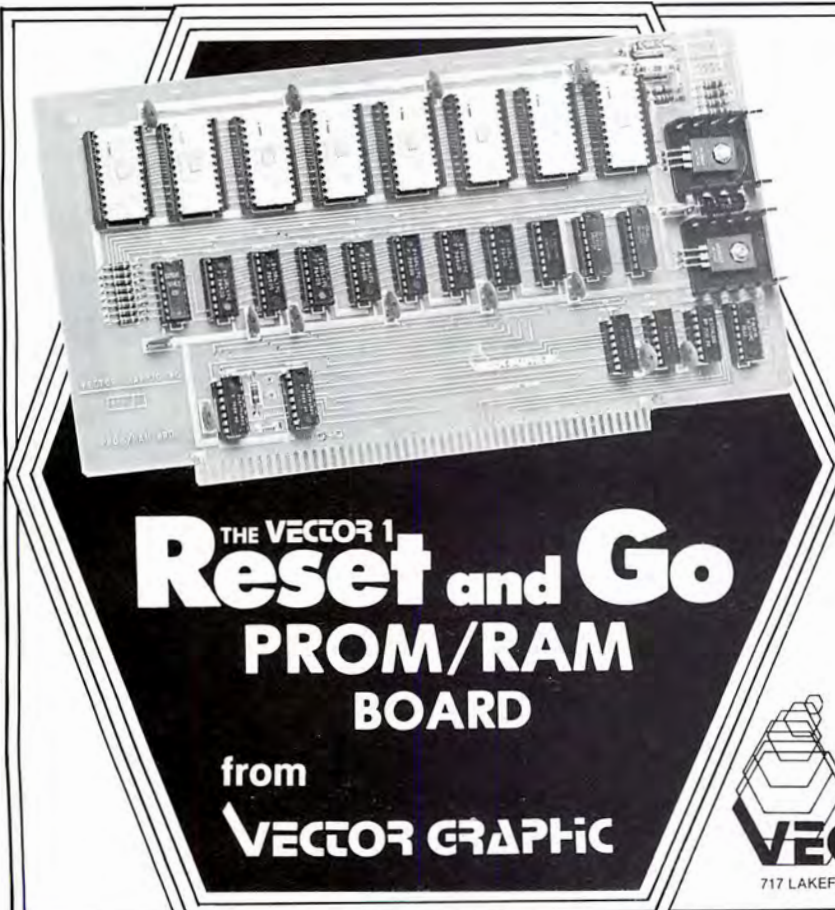
2. *The Stock Options Manual* by Gary L. Gastineau (McGraw-Hill). Another good book for the student of options. He introduces some probability theory into evaluation of options as well as graphically displaying various *hedging* strategies.
3. *How the Experts Beat the Market* by Thomas Noddings (Dow Jones-Irwin). Not for the beginner in options. He presents numerous *hedging* strategies using convertible bonds, warrants, and options.

DISCLAIMER (MY HEDGE)

The charts, tables, and examples presented in this article are for illustration only, and should not be construed as recommendations for purchase and/or sale of any individual stocks or related options. Further, it is not intended to indicate nor imply in any manner that the methods described in this article can guarantee profitable results in the future.

EXPLANATION OF PROGRAM

The program is highly modularized in design, that is, each function is processed by a separate, independent group of statements. By using this method, the basic program can be set up and expanded a piece at a time. Conversely, whole modules could be "lifted" and used without modification.



PROM: Space for 2K bytes, 1702A. Store bootstrap loaders and monitors.

RAM: 1K bytes, 2102LIPC, 450 ns, low power. NO NEED TO RELOCATE STACK WHEN ADDING MEMORY.

CIRCUITRY: Replaces memory write logic on ALTAIR™ and Imsai front panels.

REGULATORS: Two regulators. No need for regulated power supply.

JUMP-ON-RESET: PROM program execution starts at any location in memory without interfering with programs in any other portion of memory.

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OPTIONAL FIRMWARE: 512 byte monitor for use with Tarbell tape interface on 2, 1702A PROMs.

PROM/RAM KIT WITHOUT PROMS	\$ 89
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+ OPTION C - SIO 2 (IMSAI)	\$129
+ OPTION D - Poly Video Interface (Includes Video Driver)	\$159

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THE VECTOR 1

Reset and Go

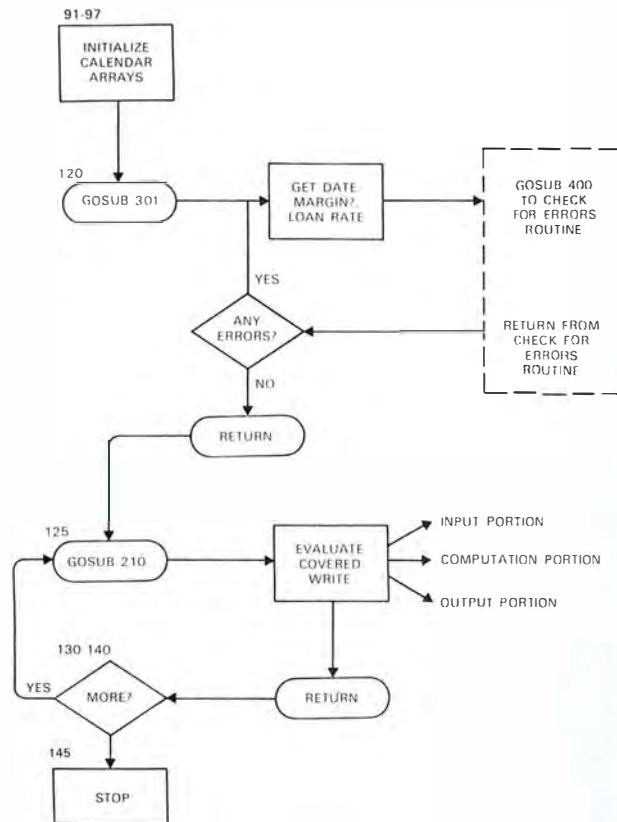
PROM/RAM BOARD

from

VECTOR GRAPHIC

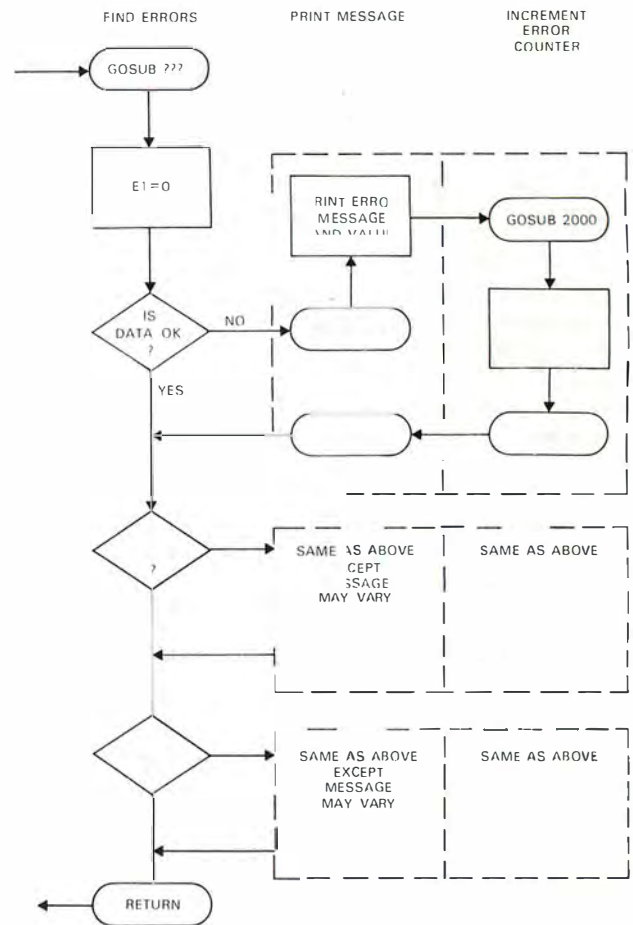
There are several features worth noting. First, liberal use of comments will help clarify the purpose of a module. Second, the error checking routines are extensive. In addition, the reason for the error or the allowable range of the value is displayed as well as the erroneous value. Third, the style of programming is made as consistent as possible. For example, extensive use of the GOSUB-RETURN statements allow the main program logic to remain in sequence. When a task must be done, the program GOSUB's to the task and RETURN's when it is done.

Fourth, GOTO statements were not used. In a few cases, the IF - THEN (go to) is used to move program control to reinitiate an input request or branch to a return statement.



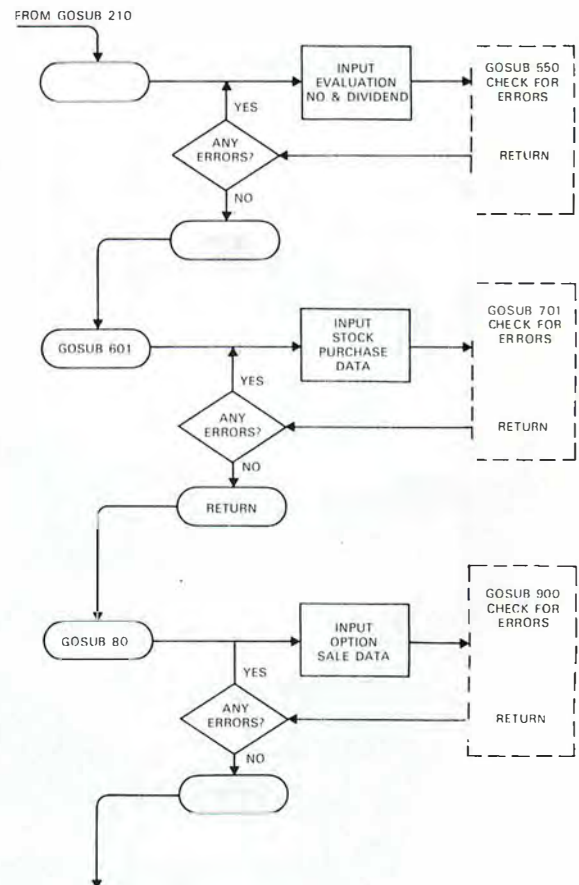
Main Program — Overview

Figure A



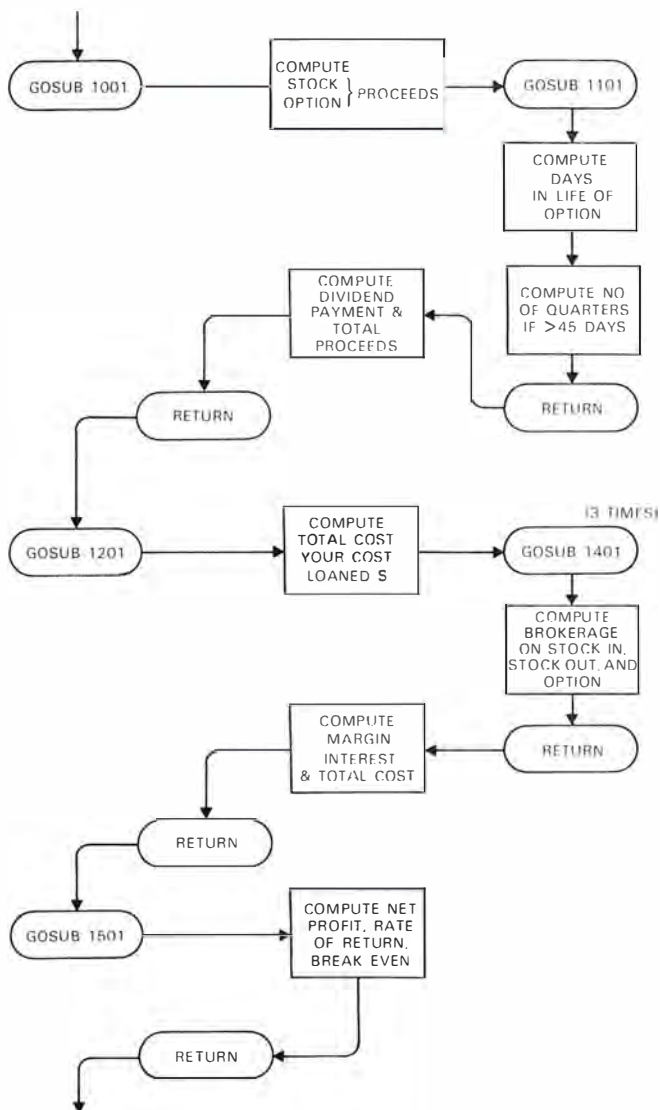
Check for Errors Routine

Figure B



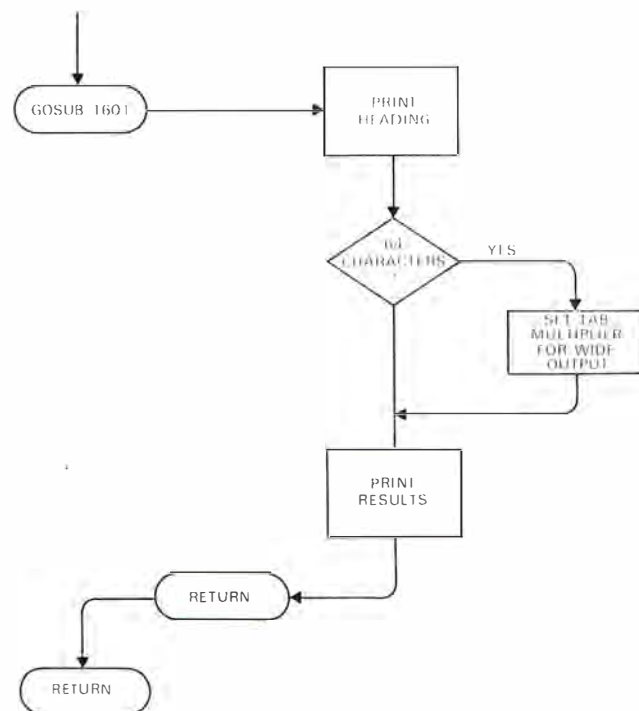
Evaluate Covered Write-Input Portions

Figure C



Evaluate Covered Write-Computation

Figure D



Evaluate Covered Write-Output

Figure E

Example. Demonstration of Extensive Edits

RUN

INPUT MM,DD,YY, MARGIN? (1=YES), LOAN RATE (###)

?76,0,0,4,3.70

DATE ERROR 76 0 0

DATE ERROR 76 0 0

INPUT MM,DD,YY, MARGIN? (1=YES), LOAN RATE (###)

?76,0,0,1,3.0

DATE ERROR 76 0 0

DATE ERROR 76 0 0

RANGE=5 TO 14% 3

INPUT MM,DD,YY, MARGIN? (1=YES), LOAN RATE (###)

?12,10,76,1,7.5

OUTPUT TO BE 32 OR 64 CHARACTERS?

?32

EVALUATION NO, DIVIDEND (\$/SHARE/QTR)

?100,6

DIVIDEND RANGE IS 0 TO \$5 6

EVALUATION NO, DIVIDEND (\$/SHARE/QTR)

?100,.08

NO. SHARES, PRICE/SHARE, MARKET(1=NYSE, 2=OTC)

?125,38.87,3

NOT EVEN 100'S 125

EXCHANGE IS 1 OR 2 3

NO. SHARES, PRICE/SHARE, MARKET(1=NYSE, 2=OTC)

?200,38.87,2

EXPIRATION MONTH, STRIKE, COST/OPTION

?0,0,0

MONTH ERROR 0

STRIKE <10 OR >3000

PRICE < \$25 0

EXPIRATION MONTH, STRIKE, COST/OPTION

?4,40,287

COVERED WRITE NO 100 12 10 76

BUY 200 SHARES AT 38.87

SELL 2 4 40 'S AT \$ 287 EACH

	COST	PROCEEDS	RETURN
YOUR \$	3887	STOCK 8000	\$ 609.0N
LOAN \$	3887	OPTION 574	3504 IS
BROKER'S		DIVIDEND 16	17.3 %
IN	42		131 DAYS
OUT	42		= 48.2 %
OPTION	32		ANNUALLY
MARGIN	91		BRK-EVEN
	-----	-----	IS
TOTALS	7981	8590	\$ 35.8

MORE? (1=YES)

?0

STOP IN LINE 145

READY

```

10 REM STOCK MARKET HEDGE - COVERED WRITING STRATEGY
20 REM WRITTEN BY EDWARD CHRISTIANSON 12/15/76
90 DIM C(12) ; REM SET UP JULIAN DATE ARRAY'
91 DATA 0,31,59,90,120,151,182,212,243,273,304,334
92 FOR I=1 TO 12: READ C(I) ; NEXT I
95 DIM M(12) ; REM SET UP MONTH DESCRIPTIONS'
97 FOR I=1 TO 12: M(I)=I; NEXT I
120 GOSUB 301; REM SET UP INITIAL VALUES'
125 GOSUB 210; REM GET INPUT DATA AND EVALUATE POSITION'
130 PRINT"MORE? (1=YES)";
135 INPUT A1
140 IF A1=1 THEN 125
145 STOP
210 GOSUB 501; REM GET STOCK DESCRIPTION AND DIVIDENDS'
220 GOSUB 601; REM GET STOCK PURCHASE DATA'
230 GOSUB 801; REM GET OPTION SALE SIDE DATA'
240 GOSUB 1001; REM COMPUTE TOTAL PROCEEDS IF CALLED'
250 GOSUB 1201; REM COMPUTE TOTAL COSTS'
260 GOSUB 1501; REM COMPUTE NET PROFITS, RATE OF RETURN'
270 GOSUB 1601; REM DISPLAY RESULTS'
280 RETURN
301 PRINT"INPUT MM,DD,YY, MARGIN? (1=YES), LOAN RATE (###)"
  
```



```

305 INPUT M,D,Y,M3,R
306 M1=1
310 GOSUB 400; REM CHECK FOR 0BVIOUS INPUT ERRORS
315 IF E1 > 0 THEN 301
320 PRINT"OUTPUT TO BE 32 OR 64 CHARACTERS? ",
325 INPUT W1
330 RETURN
400 E1 = 0; REM E1 IS AN ERROR FLAG'
403 IF M<1 THEN GOSUB 450
406 IF M>12 THEN GOSUB 450
409 IF D<1 THEN GOSUB 450
412 IF D>31 THEN GOSUB 450
415 IF Y<0 THEN GOSUB 450
418 IF Y>99 THEN GOSUB 450
421 IF M3<>1 THEN 440; REM NOT MARGINED'
424 M1=5; REM SET TO 50% RATE'
427 IF R<5 THEN GOSUB 455
430 IF R>14 THEN GOSUB 455
440 RETURN
450 PRINT"DATE ERROR ",M,D,Y
451 GOSUB 2000
452 RETURN
455 PRINT"RANGE=5 TO 14% ",R
456 GOSUB 2000
457 RETURN
501 PRINT"EVALUATION NO, DIVIDEND ($/SHARE/QTR)"
505 INPUT N9,D1
510 GOSUB 550; REM CHECK FOR 0BVIOUS ERRORS'
515 IF E1 > 0 THEN 501
520 RETURN
550 E1 = 0
551 IF D1<0 THEN GOSUB 575
554 IF D1>5 THEN GOSUB 575
560 RETURN
575 PRINT"DIVIDEND RANGE IS 0 TO $5 ",D1
576 GOSUB 2000
577 RETURN
601 PRINT"N0. SHARES,PRICE/SHARE,MARKET(1=NYSE,2=OTC)"
605 INPUT S1,P1,M9
610 GOSUB 701; REM CHECK FOR ERRORS'
615 IF E1 > 0 THEN 601
620 RETURN
701 E1 = 0; REM EDIT STOCK DATA'
706 IF S1<100 THEN GOSUB 751
709 S9=INT(S1/100)
712 IF S1<>S9*100 THEN GOSUB 751
715 IF P1<10 THEN GOSUB 755
718 IF P1>300 THEN GOSUB 755
721 M9=INT(M9)
724 IF M9<1 THEN GOSUB 760
727 IF M9>2 THEN GOSUB 760
730 RETURN
751 PRINT"NOT EVEN 100'S ",S1
752 GOSUB 2000
753 RETURN
755 PRINT"PRICE<10 OR >300 ",P1
756 GOSUB 2000

```

```

757 RETURN
760 PRINT"EXCHANGE IS 1 OR 2 ",M9
761 GOSUB 2000
762 RETURN
801 PRINT"EXPIRATION MONTH, STRIKE, COST/OPTION"
805 INPUT M6,S6,P6
810 GOSUB 900; REM CHECK FOR ERRORS'
815 IF E1>0 THEN 801
820 RETURN
900 E1=0
903 06=S1/100; REM COMPUTE NO.OPTIONS'
906 IF M6<1 THEN GOSUB 955
909 IF M6>12 THEN GOSUB 955
912 IF S6<10 THEN GOSUB 960
915 IF S6>300 THEN GOSUB 960
918 IF P6<25 THEN GOSUB 965
930 RETURN
955 PRINT"MONTH ERROR ",M6
956 GOSUB 2000
957 RETURN
960 PRINT"STRIKE <10 OR >300",S6
961 GOSUB 2000
962 RETURN
965 PRINT"PRICE < $25 ",P6
966 GOSUB 2000
967 RETURN
1001 T1=INT(06*100*S6); REM COMPUTE PROCEEDS IF CALLED'
1005 T2=INT(06*P6); REM COMPUTE OPTION PROCEEDS'
1010 GOSUB 1101; REM COMPUTE DAYS IN LIFE AND # OF QTRS'
1015 T3=INT(D1*S1*Q); REM TOTAL DIVIDEND INCOME'
1020 T4=T1+T2+T3; REM COMPUTE TOTAL INCOME'
1025 RETURN
1101 Y1=Y*365; REM COMPUTE DAYS IN LIFE'
1105 D2=C(M)+D+Y1
1110 D3=C(M6)+20+Y1; REM ASSUME OPTION EXPIRES ON 20TH DAY'
1115 D4=D3-D2
1120 IF D4<0 THEN D4=D4+365
1125 Q=INT((D4/90)+.5); REM COMPUTE QUARTERS FOR DIVIDENDS'
1130 RETURN
1201 C1=INT(S1*P1); REM COMPUTE TOTAL COST'
1205 C2=INT(C1*M1); REM C2 IS OWN CAPITAL'
1210 C3=C1-C2
1215 M8=M9; REM M8 IS MARKET TYPE FOR BROKERAGE CALCULATION'
1220 X=C1
1225 X1=S1/100
1230 GOSUB 1401; REM COMPUTE BROKERAGE ON SHARES'
1235 B1=B; REM B IS RETURNED VALUE OF BROKERAGE FEE'
1240 X=X-T1
1245 X1=S1/100
1250 GOSUB 1401; REM COMPUTE BROKERAGE ON SHARE WHEN CALLED'
1255 B2=B
1260 X=X-T2
1265 X1=06
1270 M8=3; REM M8=3 MEANS CBOE'
1275 GOSUB 1401; REM COMPUTE BROKERAGE ON OPTION SALE'
1280 B3=B
1285 C4=C3-T2-T3+B1+B2+B3; REM C4 IS NET CAPITAL BORROWED'
1290 M2=INT((C4/100)*C4)*D4/365; REM MARGIN INTEREST COST'
1291 IF M1=1 THEN M2=0; REM NO INTEREST'
1292 C5=C2+C3+B1+B2+B3+M2; REM C5 IS TOTAL COST'
1295 RETURN
1401 B=(X*.009)+22)+(X1*6); REM OLD BROKERAGE FEES'
1405 IF M8=1 THEN B=INT(B*.7); REM NYSE DISCOUNT'
1410 IF M8=2 THEN B=X1*21; REM OTC COST'
1415 IF M8=3 THEN B=INT(B*.82); REM CBOE'
1420 IF B<25 THEN B=25; REM MINIMUM BROKERAGE'
1425 RETURN
1501 N1=T4-C5; REM COMPUTE PROFIT AND RATE OF RETURN'
1505 C6=C2-T2-T3+B1+B2+B3+M2; REM C6 IS NET CAPITAL'
1510 R1=INT((N1*1000)/C6)/10
1515 R2=INT(3650*R1/D4)/10
1520 R3=(INT((C1-N1)*100)/S1)/100; REM LOWER BREAK-EVEN'
1525 RETURN
1601 PRINT"COVERED WRITE NO",N9,M,D,Y
1605 PRINT"BUY",S1," SHARES AT",P1
1610 PRINT"SELL",06," ",M(M6),S6,"$S AT $",P6,"EACH"
1611 PRINT
1614 W2=1
1615 IF W1>60 THEN W2=1.9
1616 PRINT TAB(4*W2),"COST",TAB(13*W2),"PROCEEDS",
1617 PRINT TAB(W2*24),"RETURN"
1618 PRINT"Y0UR $",C2,TAB(W2*12),
1620 PRINT"STOCK ",T1,TAB(W2*23),"$",
1622 PRINTN1,"ON"
1624 PRINT"L0AN $",C3,TAB(W2*12),
1626 PRINT"OPTI0N ",T2,TAB(W2*23),
1628 PRINTINT(C6),"IS"
1630 PRINT"BROKER'S",TAB(W2*12),
1632 PRINT"DIVIDEND",T3,TAB(W2*23),X1,X,R1,"X",X1
1634 PRINT" IN ",B1,TAB(W2*23),
1636 PRINTD4,"DAYS"
1638 PRINT" OUT ",B2,TAB(W2*23),
1640 PRINT" =",R2,"%"
1642 PRINT" OPTI0N ",B3,TAB(W2*23),
1644 PRINT" ANNUALLY"
1646 PRINT"MARGIN ",M2,TAB(W2*23),
1648 PRINT" BRK-EVEN"
1649 PRINTTAB(6),"-----",TAB(W2*12)," -----",TAB(W2*23),
1650 PRINT" IS"
1652 PRINT"TOTALS",C5,TAB(W2*12)," ",T4,TAB(W2*23),
1654 PRINT" $",(INT(R3*10))/10
1660 RETURN
2000 E1=E1+1
2001 RETURN

```

19" RACK S-100 BUS CARD CAGE



8,192 x 8 BIT STATIC MEMORY

Exceptionally Low Power



FAST

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PROTOTYPING BOARD	Z80 - CPU
EXTENDER CARD	16K RAM
2K RAM / 2K ROM	EDGE CONNECTORS
LOW PROFILE IC SOCKETS	DB25 CONNECTORS

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MERLIN's Super Dense Graphics is an add-on board which mounts directly to the MERLIN Video Interface. Each of 64,000 graphic dots is **individually** controllable and located **on-screen**. The kit includes a manual with X-Y coordinate transformation software listing.

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MERLIN Manual	\$ 10.00
MERLIN Kit	\$269.00
MEI ROM	\$ 34.95
Cassette I/O Add-on	\$ 29.00

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WARP FACTORS

**Captain's Log: Star Date 3814. 2:
Quadrant 14-Z2 Sector A-11; in po-
lar orbit around third planet, Tellian
system...**

"and all corrections have been made in the warp mechanisms at this remote site. Operations are satisfactory now. Fortunately, this planet is uninhabited — no telling how much havoc the warp forces could have caused to organic life."

"I close this entry with the narrative of a baffling discovery we made just before beaming up."

"Kkkhh? Archie? Where are you? Let's go."

"I believe Mr. Tyson is inspecting the null zone area behind the flux modulators, Captain."

"Aye, Captain; could you and Mr. Kkkhh come over here? I've found something."

"Okay, Archie, what is it? Some residual temporal perturbation still in the area?"

"No, Captain, nothing like that. See here, in the sand — some kind of apparatus that is not a part of the flux modulators, or any other system at this site."

"Let's have a look."

"Well, Mr. Kkkhh, any ideas?"

"Interesting, Captain. The printed text on this apparatus appears to be in an archaic form of English."

"H'mm, yes, I see what you mean. Educator two microcomputer HEP kit by Motorola, if I interpret correctly."

"Captain?"

"Yes, Mr. Tyson?"

"I've scanned engineering references in the ship's archives many times, but I've na' come across a heading called 'microcomputer.'"

"Perhaps, Mr. Tyson, you did not access the references in a thorough manner."

"Your ears! Mr. Kkkhh!"

"Gentlemen! Time to beam up. Bring the unit along, we'll have Computer do an analysis."

"Computer."

"Working."

"Identify the purpose, origin and age of this unit."

"Unit is a microcomputer, a primitive ancestor of myself. Point of origin, Earth circa late 1900s, Earth calendar. Age, less than thirty days old."

"What?!!"

"Easy, Archie. Computer:elaborate."

"Unit is the Educator II, a stored-program, general-purpose digital computer kit that was offered by the HEP/MRO department of an organization known as

Motorola. A block diagram of the unit is contained in my memory banks."

"Computer, display the diagram; continue the description."

"Yes, Captain. The unit contains M6800 microcomputer products. Specifically, a HEP C4801L microprocessing unit (MPU), a C4821L Peripheral Interface Adapter (PIA) and a C4811L 128x8 Random Access Memory (RAM). There are provisions on the single board kit for another 128x8 RAM. A built-in interface allows additional user programs to be stored on and loaded from audio cassette tapes. User programs on cassettes may be accessed and loaded into RAM by means of a software search feature. Said interface and search features are routines contained in Programmable Read Only Memories (PROMs) on the board. The two 512x4 PROMs also contain an executive monitor for user/computer interaction by means of front panel switches and a light emitting diode (LED) display. A clock circuit, running at 0.5 MHz, is also on-board. The unit is self-contained; all parts are included as well as a complete construction manual. The unit requires a 5 V, 1.2 A power source."

"Computer, what other modes of communication were available to the users of this Educator II?"

"At the point in time when this unit was introduced, Mr. Kkkhh, tactile/visual interaction was in vogue. Verbal interaction was in its infancy."

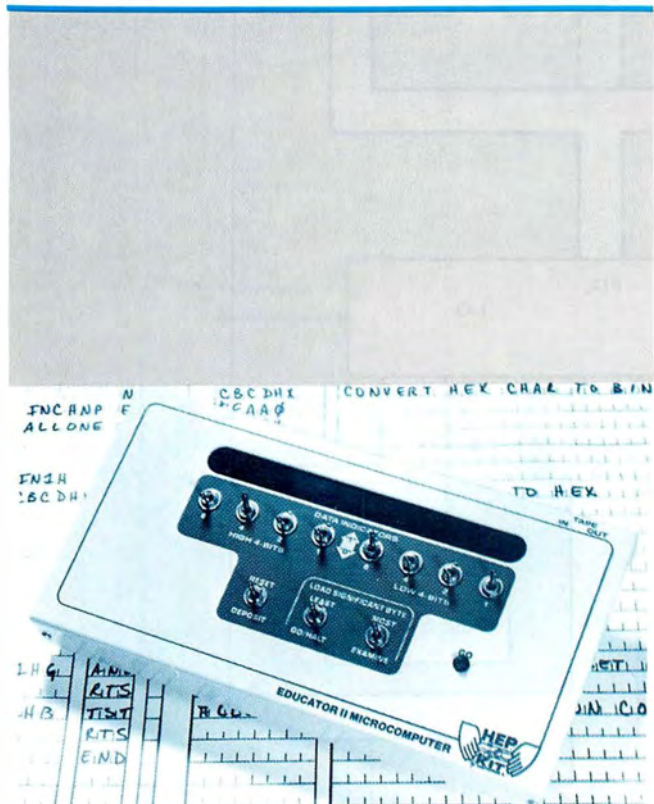
"Highly interesting. Computer, how was this tactile/visual communication implemented?"

"User/computer dialogue was at the machine code level for the initial Educator II kit. Object code patterns were set by means of eight single pole, double throw switches (SPDT) and loaded, examined and modified by three SPDT momentary switches. Bytes of code were displayed on eight LEDs. Subsequent Motorola products and user system expansions produced highly articulate configurations."

"Computer, continue with the description of the Educator II."

"Yes, Captain. Edge connectors on the board provide an interface to the PIA as well as all address, data and control bus signals for system expansion. A

**At technology Level 8
great strides were
made in microcomputing**



Educator II Microcomputer

**Do those aboard the ancient
vessels in Space know
what they contributed?**

test-as-you-build approach provided for an accurate, low-error kit construction. Assembly time was typically one Earth evening. A complete construction manual as well as a full complement of parts helped to hold the assembly time to such short duration. Tutorial support documentation, designed as aids for understanding MPUs and programming concepts, was also included. Shortly after Educator II's introduction, other HEP support kits, such as a power supply and memory boards, were also introduced."

"All well and good, but, Captain, we still ha' one verry perplexin' question: How can something from the 20th century, Earth, cross par-secs of space and still be new?"

"Yes, Archie, perplexing, true; but not entirely improbable, eh, Kkkhh?"

"Quite plausible, Captain."

"Computer, state the particulars of Educator II's introduction."

"Educator II Microcomputer Kit introduced March 1977, Earth calendar. Place of manufacture: northern hemisphere of Earth, in the country then known as the United States of America, in the State then known as Arizona. When this culture reached technological Level 8, this manufacturer identified as Motorola, Inc. maintained a lead in the design and application of signal technology."

"Does that suggest anything to you, Mr. Kkkhh?"

"The factors are favorable . . . simplicity, economy, availability. Yes, given such a potential target area, the probability of exchange would indeed be high. There is, of course, only one way to enforce this hypothesis, Captain."

"Do the honors, Mr. Kkkhh."

"Computer."

"Working."

"Computer, state the occurrence and periods of spatial alignments of Earth and Tellian III between January, 1977, Earth calendar, and Star Date 3814.2. Specify Star Date."

"Occurrence: 1977.5; 2995.84; 3814.13; Period: 35 Star Hours aligned, 140 Star Hours non-aligned. Fifty-two pulses per occurrence."

"H'mmm; yes, highly probable, Captain. An exchange could occur again at a conjugate site."

"Agreed Archie, take this Educator II and beam it down to the location that is diametrically opposite to the location at which you found it."

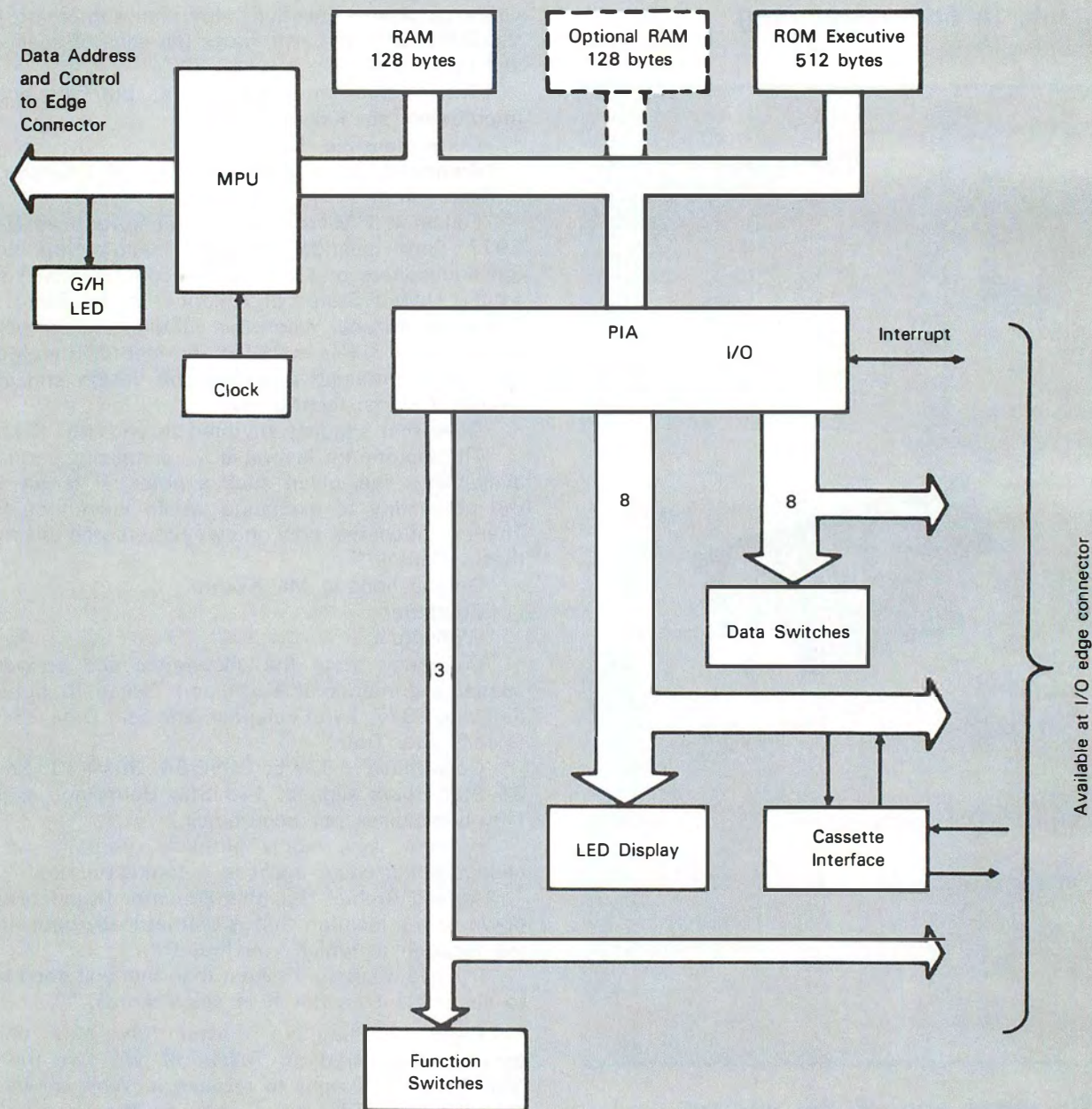
"Uh, aye, Captain. I take it then that you don't want to keep this Educator II in ships stores?"

"Right, Archie. No matter how this microcomputer appeared on Tellian III, we owe the original owner the right to retrieve it. Who knows but that this, this Educator II may be the seed bed of ideas that led to our computer."

"Aye, Captain."

"Mr. Ooll, lay in a course to Digitus IV, warp factor five."

"Aye, aye, Captain."



HEP Educator II Systems Block Diagram

Apple Introduces the First Low Cost Microcomputer System with a Video Terminal and 8K Bytes of RAM on a Single PC Card.

The Apple Computer. A truly complete microcomputer system on a single PC board. Based on the MOS Technology 6502 microprocessor, the Apple also has a built-in video terminal and sockets for 8K bytes of on-board RAM memory. With the addition of a keyboard and video monitor, you'll have an extremely powerful computer system that can be used for anything from developing programs to playing games or running BASIC.

Combining the computer, video terminal and dynamic memory on a single board has resulted in a large reduction in chip count, which means more reliability and lowered cost. Since the Apple comes fully assembled, tested & burned-in and has a complete power supply on-board, initial set-up is essentially "hassle free" and you can be running within minutes. At \$666.66 (including 4K bytes RAM!) it opens many new possibilities for users and systems manufacturers.

You Don't Need an Expensive Teletype.

Using the built-in video terminal and keyboard interface, you avoid all the expense, noise and maintenance associated with a teletype. And the Apple video terminal is six times faster than a teletype, which means more throughput and less waiting. The Apple connects directly to a video monitor (or home TV with an inexpensive RF modulator) and displays 960 easy to read characters in 24 rows of 40 characters per line with automatic scrolling. The video display section contains its own 1K bytes of memory, so all the RAM memory is available for user programs. And the

Keyboard Interface lets you use almost any ASCII-encoded keyboard.

The Apple Computer makes it possible for many people with limited budgets to step up to a video terminal as an I/O device for their computer.

No More Switches, No More Lights.

Compared to switches and LED's, a video terminal can display vast amounts of information simultaneously. The Apple video terminal can display the contents of 192 memory locations at once on the screen. And the firmware in PROMS enables you to enter, display and debug programs (all in hex) from the keyboard, rendering a front panel unnecessary. The firmware also allows your programs to print characters on the display, and since you'll be looking at letters and numbers instead of just LED's, the door is open to all kinds of alphanumeric software (i.e., Games and BASIC).

8K Bytes RAM in 16 Chips!

The Apple Computer uses the new 16-pin 4K dynamic memory chips. They are faster and take 1/4 the space and power of even the low power 2102's (the memory chip that everyone else uses). That means 8K bytes in sixteen chips. It also means no more 28 amp power supplies.

The system is fully expandable to 65K via an edge connector which carries both the address and data busses, power supplies and all timing signals. All dynamic memory refreshing for both on and off-board memory is done automatically. Also, the Apple Computer can be upgraded to use the 16K chips when they become availa-

ble. That's 32K bytes on-board RAM in 16 IC's—the equivalent of 256 2102's!

A Little Cassette Board That Works!

Unlike many other cassette boards on the marketplace, ours works every time. It plugs directly into the upright connector on the main board and stands only 2" tall. And since it is very fast (1500 bits per second), you can read or write 4K bytes in about 20 seconds. All timing is done in software, which results in crystal-controlled accuracy and uniformity from unit to unit.

Unlike some other cassette interfaces which require an expensive tape recorder, the Apple Cassette Interface works reliably with almost any audio-grade cassette recorder.

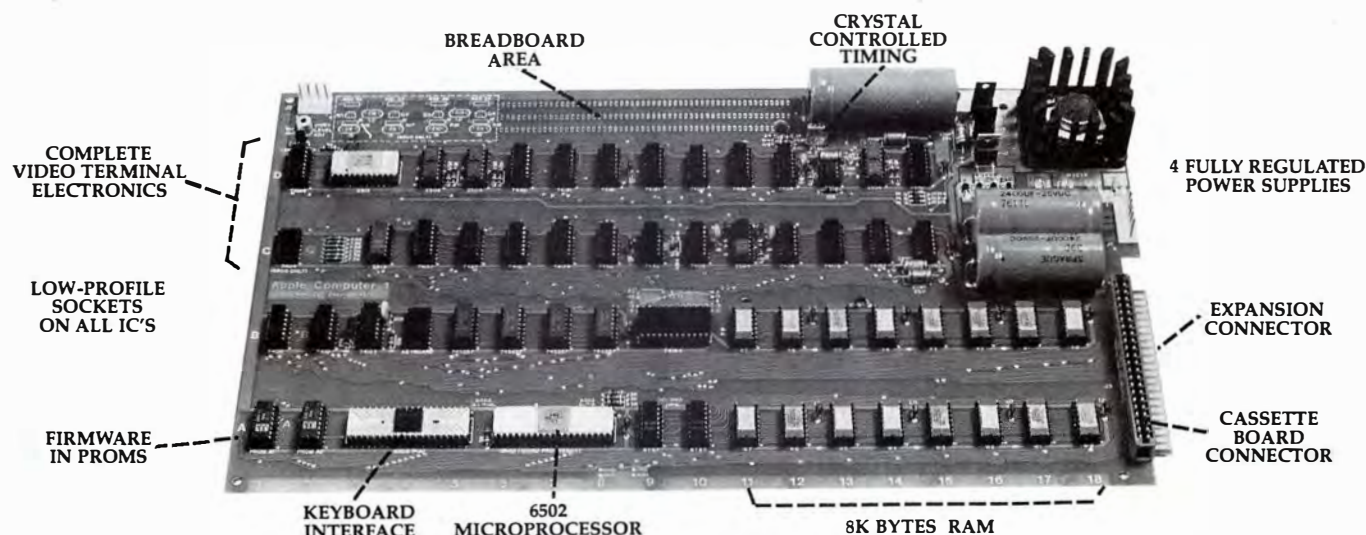
Software:

A tape of APPLE BASIC is included free with the Cassette Interface. Apple Basic features immediate error messages and fast execution, and lets you program in a higher level language immediately and without added cost. Also available **now** are a dis-assembler and many games, with many software packages, (including a macro assembler) in the works. And since our philosophy is to provide software for our machines free or at minimal cost, you won't be continually paying for access to this growing software library.

The Apple Computer is in stock at almost all major computer stores. (If your local computer store doesn't carry our products, encourage them or write us direct). **Dealer inquiries invited.**

Byte into an Apple \$666.66*

* includes 4K bytes RAM





FLIP OVER OUR FLOPPY

Only \$750 from Peripheral Vision.

Peripheral Vision is a brand-new company that's dedicated to selling reasonably priced peripherals for various manufacturers' CPU's.

We think you'll flip over our first product.

It's a full-size floppy disk for the Altair-Imsai plug-in compatible S-100 BUS. And it's available for as low as \$750.

Here are the features:

- 1 interface card supports 4 drives
- Stores over 300,000 bytes per floppy
- Bootstrap EPROM included—no more toggling or paper tape
- Completely S-100 plug-in compatible
- Interface cabling included
- Drive is from Innovex (the originator of the floppy concept)—assembled and tested
- Interface card design is licensed from Dr. Kenneth Welles and the Digital Group
- Disk operating system with file management system included on floppy
- Cabinet and power supply optional

Prices:

	Kit	Assm.
Interface card kit and assembled and tested drive	\$750	\$850
Power supply—+24V at 2A	45	65
Cabinet—Optima, blue	—	85

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BUILDING A 12-BIT ANALOG TO DIGITAL CONVERTER FOR REAL TIME PROBLEMS

By Roger W. Brown

In order to make your computer aware of its environment it is necessary to input sensory data into its memory. Since most sensory data encountered in our environment are analog in nature they must be converted to digital value before the computer can understand them. This conversion process is accomplished by using an A/D converter as an interface between your computer and the analog signal supplied.

The heart of any real world interface is an analog to digital (A/D) converter. This A/D converter functions as a translator for the various analog stimuli from the outside world converting them into computer code. The analog stimuli are first converted into analog voltages by a transducer, such as a temperature module, and then input to the A/D converter which transforms the analog signal into its respective digital value. In order to minimize cost, additional sensor modules may be connected to a multiplexer board to allow several sensors to share the same A/D converter. Likewise, the output from the computer may be converted into its analog equivalent by a digital to analog (D/A) converter. This permits the computer to do such things as drawing plots, or displaying graphics on an oscilloscope or television screen, or generating a computer voice to talk to you. Many outputs may be generated at the same time by using one D/A converter and another multiplexer board, to reverse the above multiplexer procedure.

The A/D converter will perform the actual conversion of the analog signal into a binary word, for processing by the computer. The larger the binary word the greater the resolution and the more accurately the computer will be informed about the input signal. For example, a 10 bit A/D converter set for ± 5 volt operation has 512 steps of resolution between 0 and 5 volts and 1024 steps between -5 and $+5$ volts. This amounts to a resolution of better than 0.010 volts or 10mV per step. Consequently a 12 bit unit would have resolution to 2mV. The resolution of the A/D converter best suited to your needs will depend upon your particular application. However, it is well to remember that a 16 bit unit can be used as a 10 or 8 bit A/D converter when less resolution and greater speed are required, but an 8 or 10 bit unit cannot be used as a 16 bit A/D converter.

Once you have interfaced your computer with an A/D and/or a D/A converter module you are ready to hook-up the external sensors. If more than one sensor for an A/D converter or more than one output for a D/A converter are desired, a multiplexer must be interfaced between the converter module and the outside equipments.

Uses to which you could put your computer requiring A/D conversion are extremely numerous so only a few are given here. Your computer could be used around the house to provide you with a very sophisticated fire, smoke or intruder alarm system without the false alarm flaws of other systems presently on the market. Or it can be used to monitor outside weather conditions to forewarn of the pending dangers from water pipes and car radiators freeze up. As an external temperature monitor using wind speed and pressure gauges the system can predict local weather conditions for you. If you have a desire for privacy or need security you could use your computer to scramble your phone communications. In the garage your computer can monitor the operating systems of your car. The new Volkswagens have a connector on them specifically for this purpose. Auto systems such as timing, dwell, combustion, air pressure, engine torque, cam wear, plug and wire conditions, etc. can be monitored for preventative maintenance, tune-ups, and repairs. If you do much boating your computer can keep track of your speed, time, wind and water speed. From this it can tell you your position at any time and instruct you on course change to make to reach a desired target in the least amount of time, taking drift and winds into account. Tied to a radio receiver it can function as your inertial navigation system by receiving and processing Loran or Navy satellite signals. On-board it could also serve as the processing center for side scan sonar, eliminating the costly recording and processing equipment now in use. By interfacing a microphone to your computer it could be taught to understand voice commands and with the addition of a speaker it could even talk to you. With the new MOS matrix IC's your computer could be given sight and used to monitor any room in your house. The list is endless and these are but a few uses shown here. However, to provide sight and sound functions, a very large memory would be required.

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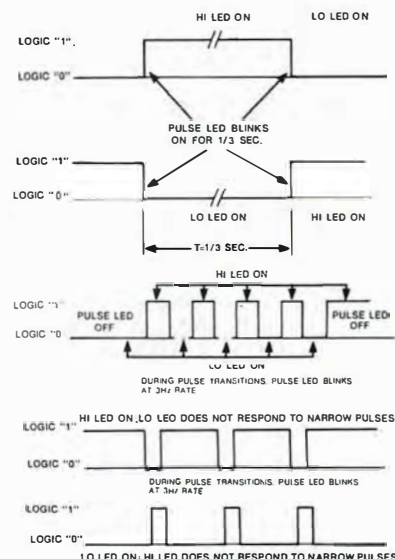
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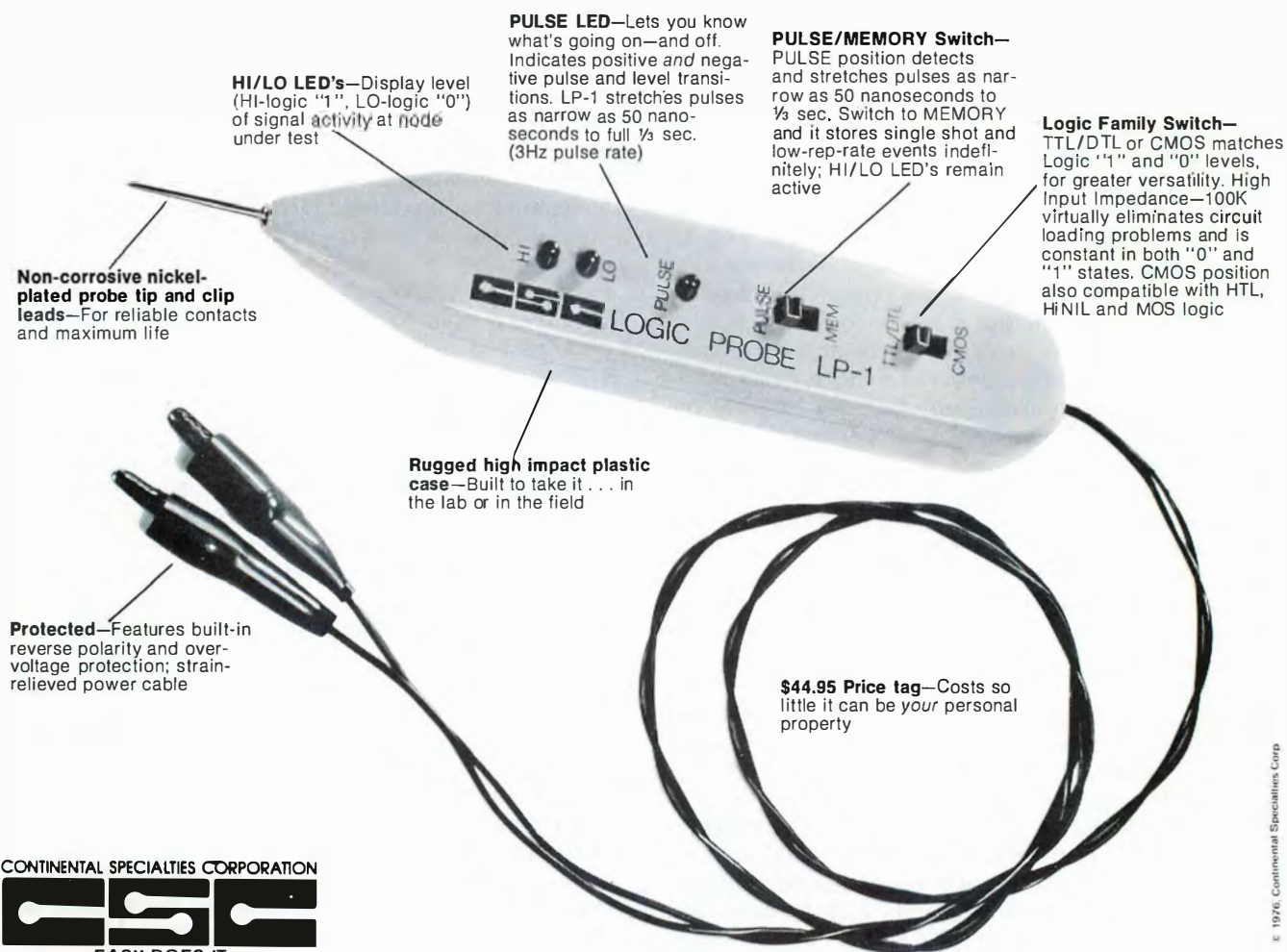
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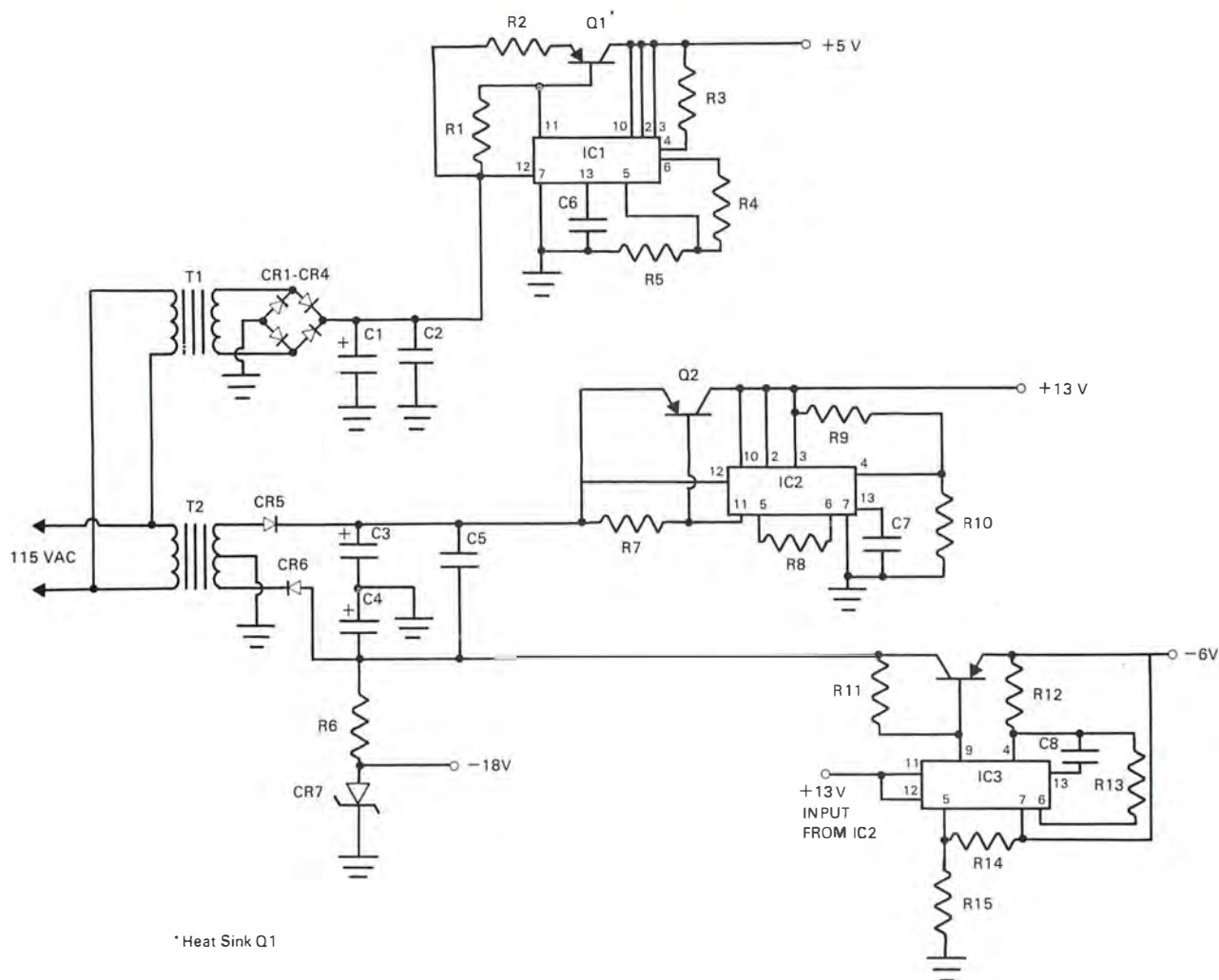
FEBRUARY 1977

ceeded, the output immediately becomes erratic and warns you of the need for adjustment. What must be done to observe signals that are faster than the slew rate of the converter is to reduce the input amplitude and you are back in business again at a decreased resolution. An additional advantage of the tracking A/D converter over the other two types discussed here is the continuous availability of data at the output of the converter.

ABOUT THE CIRCUIT:

[illegible]

FEBRUARY 1977



* Heat Sink Q1

Figure 2. Power Supply

IC5, is greater than the true input signal, the output goes positive reversing the up/down counters, IC9 through IC11. The output of IC5 after filtering out the switching transients through R18 and C10, goes to the input of IC6. The main function of IC6 is to select either IC5 for the feedback path or an optional multiplexer, the theme of a future article. In the present schematic the multiplexer input is disabled. The output from IC6 goes into IC7 along with the clock pulses from IC8. When the output of the comparator is high so is the output of IC6, then IC7 forces the up/down counters to count down. This continues until the comparator output goes low, at which time IC7 causes the counters to count up. This process is repeated quite rapidly as the clock is operating at about 10MHz. The clock pulses are generated from IC8 with R19, R20 and C11 as passive feedback elements in a TTL loop. These could be replaced by a crystal if a specific operating frequency is desired. The operations of the up/down counters are used to exercise the two 6 bit D/A converters and generate the binary coding. These two D/As, IC12 and IC13, are the heart of the system. Each converts its binary input to an equivalent analog voltage. The analog voltages of each D/A is summed, using different weighting functions by IC14. C12 is used to remove any switching noise that may have reached the converters. R25 is used to adjust the maximum input voltage range, peak to peak. R30 is used for adjusting the A/D for bipolar or biased operations.

The output of IC14 is returned to IC5 where it is compared to the input signal and the cycle starts again.

CONSTRUCTION

Component placement is not critical. Make certain the diodes and electrolytic capacitors are properly connected and their polarity is arrested. Use a 40 watt or less soldering iron with fine resin core solder. Apply only enough heat to assure a good connection. All of the parts are standard consumer grade parts. With the exception of R23 and R24 none of the parts is critical and substitutions may be made. All resistors are 20% tolerance and all capacitors are 25 volts, except where noted. For the IC's I would recommend the use of Molex Soldercons as this will eliminate the possibility of heat damage. The power supply can be assembled on the same PC board as the A/D, thus reducing the number of interconnects. The inputs and outputs may be labeled for ease of identification. This can be done with the aid of one of the inexpensive label makers on the market today. The board may be placed inside your computer and use its power supply, hence reducing the need for the two transformers and filters.

SET-UP AND CHECK-OUT

After you have completed the assembly and checked all the regulated voltages, you are ready to

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set-up the converter for real time operations. The set-up will be discussed for bipolar operations of the A/D. Other biased operations would be set-up similarly. First ground the analog input to IC4. Then adjust R30 for 5 volt output for bipolar operation, zero volts with respect to circuit ground, for positive operation only or 10 volts for negative input signals. Place a voltmeter on the output of pin #10 on IC14. The voltmeter should read zero volts, adjust R30 until it reads zero volts, within 1/10 volts or so. Adjust R25 to approximately 1100 ohms total resistance. Recheck the voltmeter and adjust R30 as above. Next, apply a +4 volt DC voltage to the analog input of IC4. Adjust R25 until the voltmeter reads +4 volts. Then ground the input and check for zero volts. If within 20mV proceed otherwise "tweak" R30. Now apply a -4 volt DC level to the input and check the voltmeter. If it doesn't indicate volts try reversing the leads; if it still doesn't indicate -4 volts adjust R25 accordingly. Repeat the zero check again and your A/D should be ready to go.

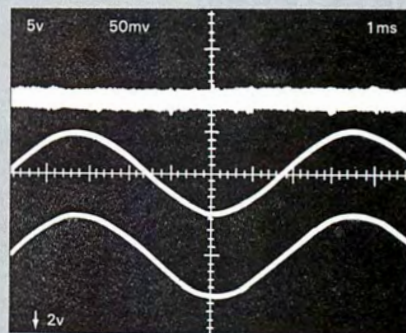
If you have an oscilloscope connect it to pin #10 of IC14 and apply an approximate 100 Hz sine wave signal with an 8 volt peak to peak level to the analog input. The scope will trace out the reconstructed input signal. Now slowly increase the frequency until the trace breaks, (see Figure 3). This is the maximum fre-

quency sine wave signal that your unit can track for an 8 volt input signal. If you reduce the signal to 1 volt and repeat this you will find the trace now tracks until the frequency has been increased to eight times what is observed for the 8 volt signal. For a 12 MHz clock the A/D can track a 1100 Hz sine wave signal and the settling time to 12 bits is less than 3 microseconds. As adjusted this 12 bit A/D offers resolution steps of 1.22 mV per bit for 5 volt bipolar operation. R25 is used to set the full scale voltage level. If its resistance is set to about 2200 ohms instead of 1100 ohms, as adjusted above, the unit will have a resolution of 0.625 mV per step but will only accept signals that deviate less than 2.5 volts about ground.

This circuit, as can be seen, offers quite a bit of flexibility in its design and operation. Its operation may be optimized to accommodate virtually any type of input signal. In addition if desired its clock and operations may be synchronized with an external clock. After you have interfaced this converter with your computer, by simply connecting the 12 digital bits to the parallel input, you are ready to hook-up a sensor and do some real time processing. Future articles will describe a multiplexer module and various sensor modules to be used with your A/D.

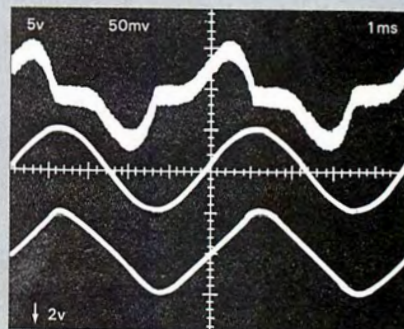
Normal Operation

Comparator Input
Analog Input
Reconstructed Analog Input



Slew Rate Limiting

Comparator Input
Analog Input
Reconstructed Analog Input



Input Over-range

Comparator Input
Analog Input
Reconstructed Analog Input

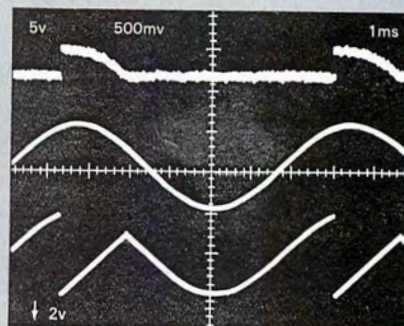
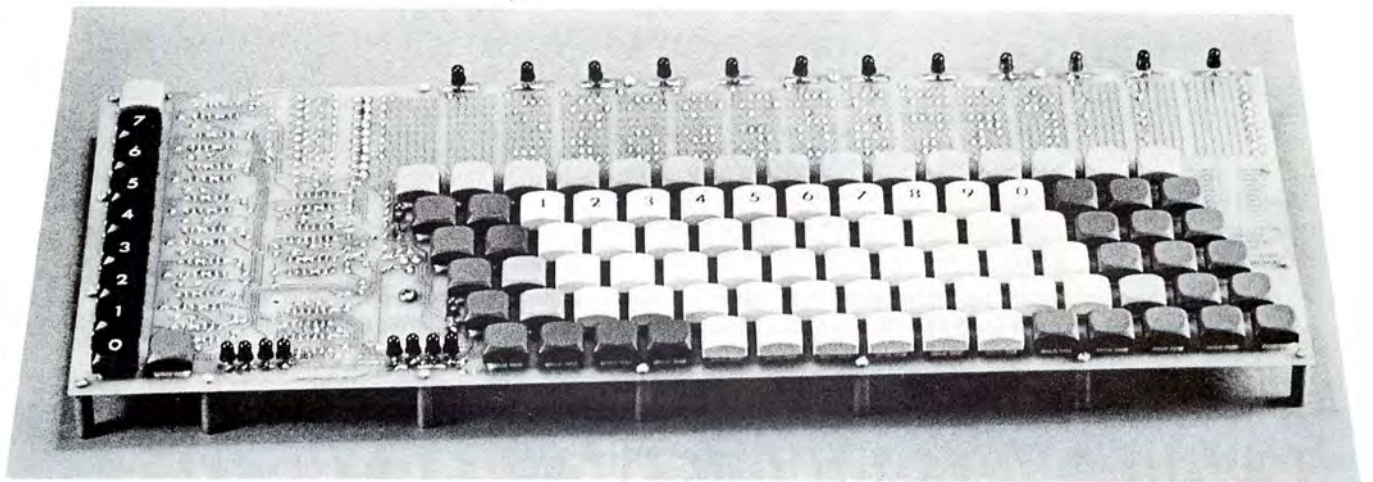


Figure 3.

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R1	270	R11	220 @ 2W	R21	220
R2	12 @ 5W	R12	3.6K	R22	220
R3	3.6K	R13	3.6K	R23	16.8K 1%
R4	5.4K	R14	3.8K	R24	1.05K 1%
R5	12.3K	R15	2.8K	R25	5K trimpot
R6	27	R16	1.1M	R26	22K
R7	150	R17	22K	R27	51K
R8	3.6K	R18	1.5K	R28	51K
R9	4.6K	R19	20	R29	51K
R10	5.1K	R20	200	R30	10K trimpot

Capacitors:

No.	Specs.	
C1, C3, C4	1000 mF @ 25V	T1 secondary 8V to 12V @ 1A
C2, C5	.01 mF	T2 secondary 24V (ct) @ at 1A
C6, C7, C8	.001 mF	CR1, CR2, CR3, CR4, CR5, CR6 1N 4006
*C9	560 pF	CR7 1N 967
*C10, C11	100 pF	
C12	1000 pF	Q1, Q2, Q3 2N 3741

IC1, IC2, IC3	#723
IC4	#741
IC5	#710
IC6, IC7, IC8	#7400
IC9, IC10, IC11	#74193
IC12, IC13	#DAC-01
IC14	#747

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Note: All of the parts excluding the misc. parts and transformers are available in kit form for \$119.50 from Scientific Research Inst.; P.O. Box 83; Marcy, NY 13403. The P.C.

Board is also available from this source for \$18.00. A P.C. Board plug compatible with the Altair 8800 is available for \$21.60.

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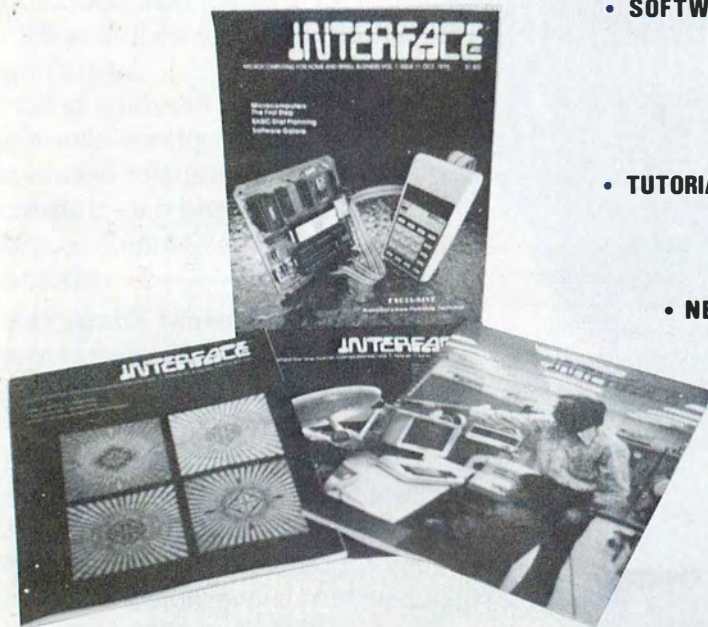
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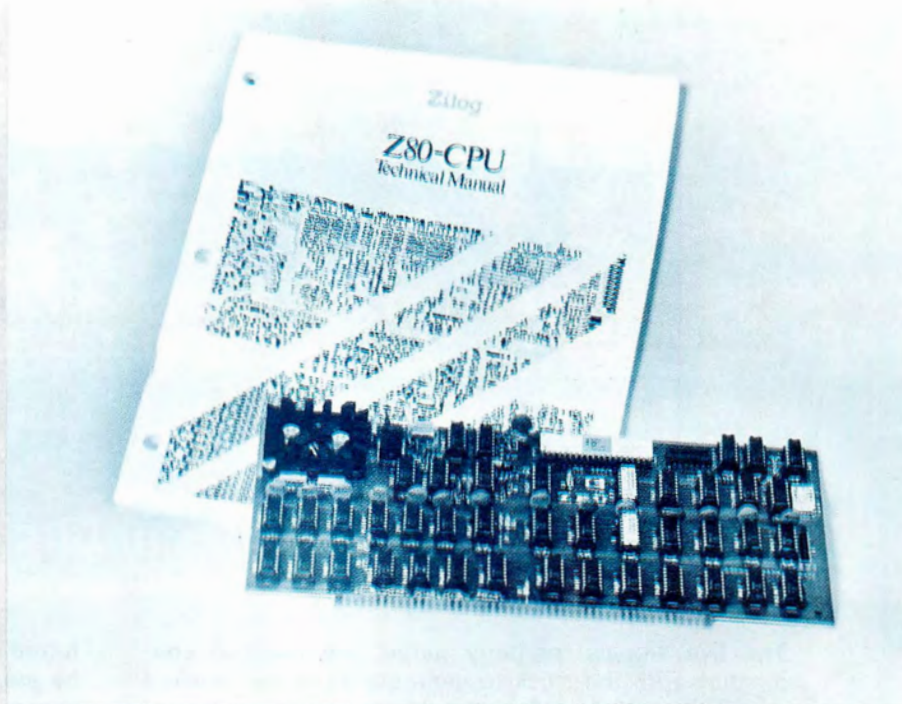
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For most people the Z-80 chip signaled the start of another learning curve in microprocessor technology while others enjoyed the start of a whole new micro-computer revolution



CARD OF THE MONTH THE TDL ZPU™

By Roger Edelson, Hardware Editor

To be fair, this article should have run before my discussion of the other available S-100 bus compatible Z-80 CPU card. The reason is simple: TDL (Technical Design Labs) were out first with their Z-80 CPU board. So this month I will cover the Z-80 CPU card from TDL. I don't know which company, TDL or Sony owns the rights to the name ZPU, nor is my intention to compare the two boards, rather to confine myself to a discussion of the TDL entry. I must say, however, that either board would be a worthwhile addition to your computer.

Let us take a look at the TDL ZPU™ kit before we cover operation and design. The kit is particularly easy to build. My son who is fourteen years of age took about three hours - with time off for ice cream. The board worked the first time out. Assembly instructions are excellent, but please read the paragraph on the identification of the electrolytic capacitor lead polarity. One of the capacitors, C 20, is very strange. It has a single big black dot located in the middle of the two leads. When the dot faces you, the right lead is the positive one. Further on this subject, let me voice a minor gripe: the capacitor is not shown on the schematic diagram. In fact none of the regulator components is shown. This makes troubleshooting this area somewhat difficult. I hope TDL redraws their schematic to include these components.

The printed circuit board is high quality with gold-plated edge-connector pins. Sockets are provided for all integrated circuits. A nice touch is the numbering of every tenth pin on the front of the board. The solder masking is generally adequate, but there were some

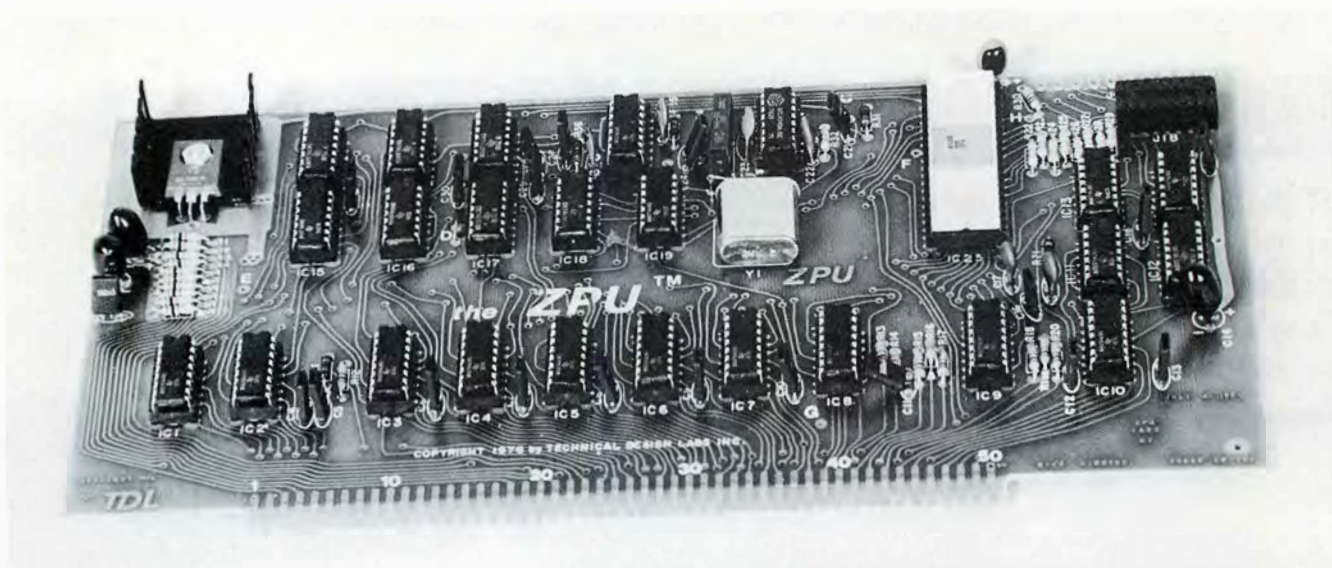
outages on the board front. Where these occurred under a silk-screened component identification, the printing did not take. It is then difficult to read the component identification. With mine most of the resistor numbers on the left side of the board vanished and some identification on the top was also lost. That was a minor problem, but does not detract from the board's construction nor use.

The assembly of the board is straightforward and easy. The assembly instructions contain a particularly good section on the proper procedure for board cleaning. The card is designed to be compatible with the S-100 bus structure or the Altair/IMSAI front panel interconnection. Separate jacks are provided to accommodate the front panel connectors of either computer, and the ZPU user may elect to install either one or both during assembly.

Now let us take a look at the general board design and the specific features provided by TDL. As stated previously, the TDL ZPU™ is S-100 bus compatible. In order to maintain this compatibility the ZPU must generate a number of bus signals not normally produced by the Z-80. The ZPU card produces these signals by logical interaction and gating of the Z-80's status signals and the clock lines.

The most important status generated by the Z-80 are:

1. Memory request
2. I/O Request
3. Read
4. Write
5. M1



The five signals, properly gated, are used in conjunction with the clock to generate all of the required control timing. To follow the description of the logical design of the ZPU, please refer to the schematic of the ZPU card shown on Figure 1.

The Z-80, unlike the 8080, outputs continuous status information whereas the 8080 information is strobed into an 8 bit latch (usually an 8212) during "Sync" time. Consequently, the Z-80 generates no sync pulse. In order to retain the Altair Bus structure, a "psuedo-sync pulse" was created.

Specifically, PSYNC is generated by gating I/O request and memory request thru a NAND gate (IC21) whose output goes to the input of a 74LS74 (IC16) which is clocked by the Phase 2 signal. PSYNC is taken off of the \bar{Q} of IC16.

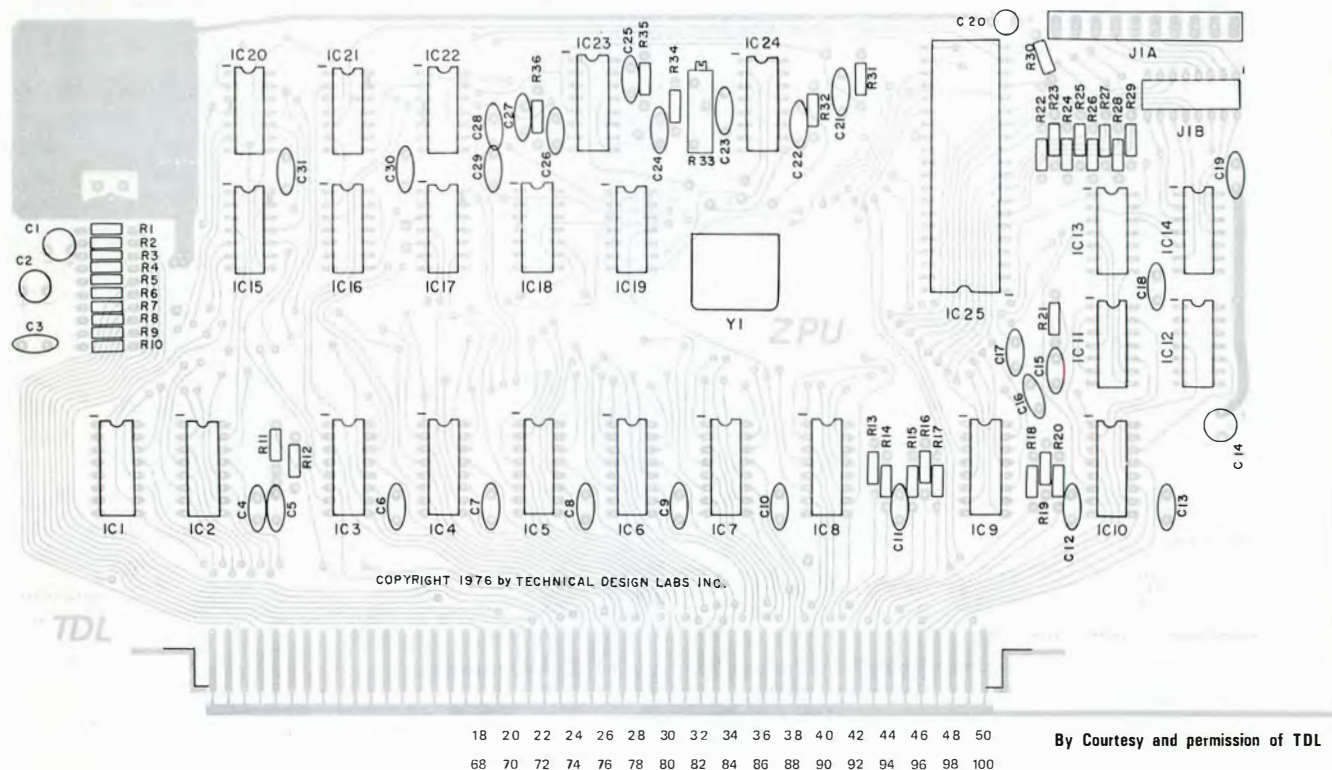
A wait is accomplished by gating the PRDY signal and forcing a low into the wait control line of the Z-80. In addition, an extra PRDY line has been made available which may be **jumpered** to any unused bus line for

future applications. When not in use these lines should be **jumpered** together. (pins # 3 and #5 of IC17) The wait signal is initiated by the coincidence of the clock pulse with the pulling down of any of the 3 ready lines (PRDY, XRDY, LRDY).

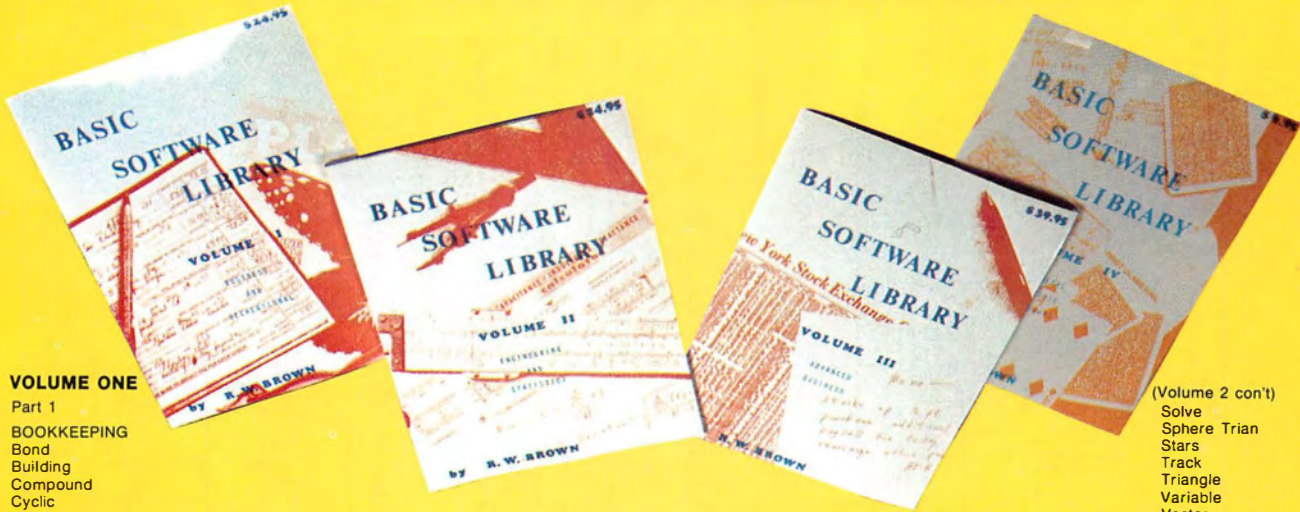
The interrupts enabled flag is not provided on the Z-80. This has been simulated by the use of an 8 input NAND gate (IC14) and some decode gating (IC17) feeding a set-reset flip flop (IC18) to provide the user with a proper indication when the interrupts are enabled.

The interrupt pin of the Z-80 is handled in exactly the same fashion as that of the 8080, coming to the same bus pin. However, the non-maskable interrupt pin of the Z-80, which represents a significant feature of the Z-80 is brought out to a pull-up resistor, and may be **jumpered** to pin #4 on the bus, $\overline{VI0}$, the highest priority interrupt line. Thus configuring the Z-80 into the Altair Bus does not detract from this Z-80 feature.

The SSTACK status signal of the 8080 is not gener-



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Variance 1
Variance 2
XY

APPENDIX A
BASIC STATEMENT DEF

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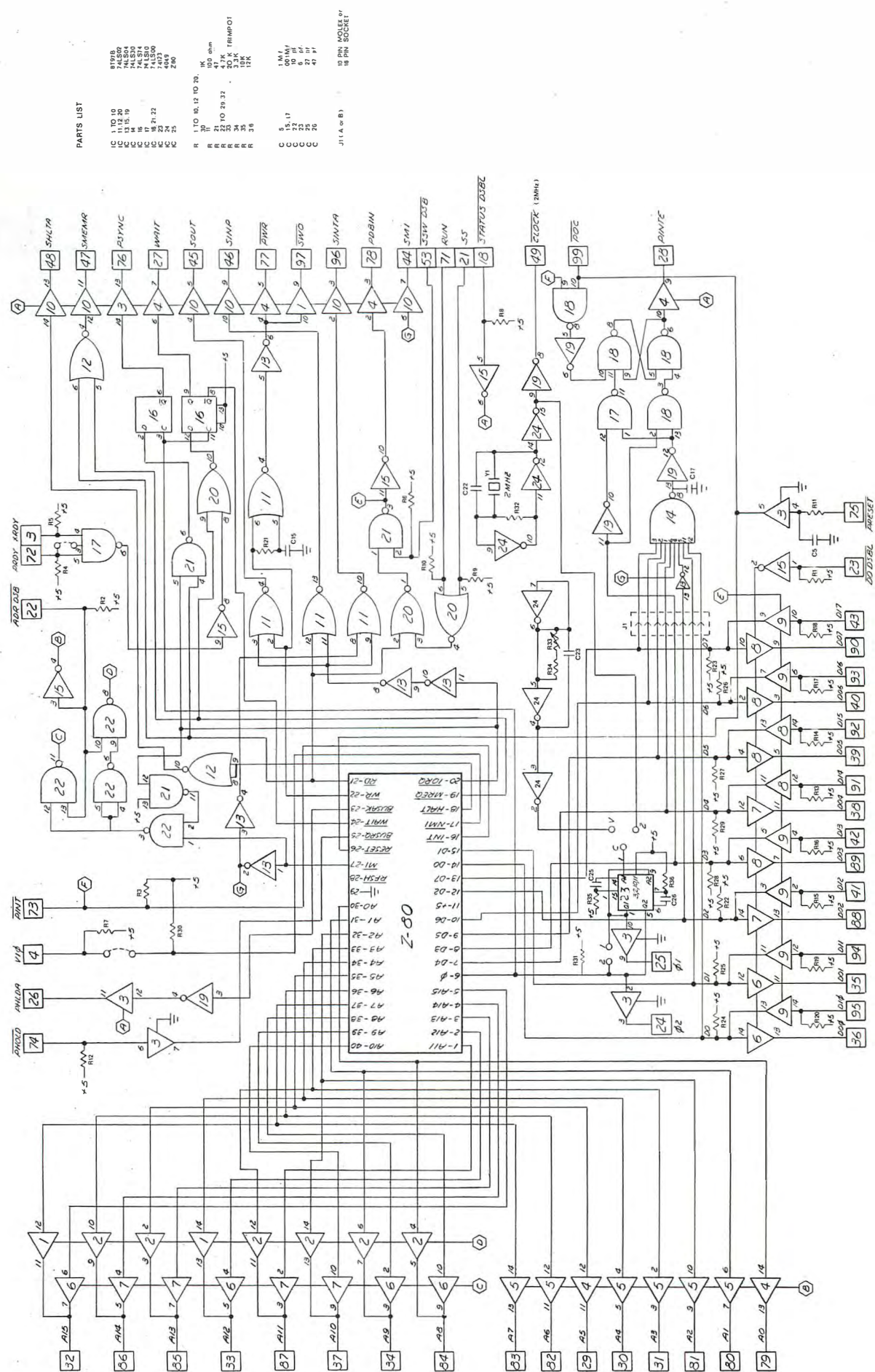
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ated. Instead, the Z-80 REFRESH signal may be **jumpered** out to this line for use with future dynamic memory designs.

Processor write is generated by the Z-80, however in this application TDL has added some additional delay in order that the STATUS OUT or MWRITE may be properly decoded.

Handling of the remaining control timing is straightforward. HALT ACK is generated by the Z-80. The MREAD signal is a function of the Z-80 READ and MREQ signals. STATUS OUTPUT is a function of WRITE in conjunction with an I/O request. STATUS INPUT is a function of a READ in conjunction with an I/O request. PDBIN is a function of the READ signal. The interrupt acknowledge signal is a function of a simultaneous MI and I/O request.

All processor signals with the exceptions of phase one, phase two, and not clock are tri-statable thru the normal Altair bus signal.

The ZPU card features two clocks on-board. The first is fixed at 2MHz thru crystal control, and the second is variable between less than 1 and greater than 4 Mhz by means of a 20 turn trimpot.

The 2Mhz crystal controlled clock is selected by placing a jumper between the augat pins labeled "C" and "2M".

The variable speed clock is selected by "jumpering" between "C" and "V". (The pins "C", "2M" and "V" are located in area A on the ZPU card.)

The crystal oscillator is a parallel resonant circuit using a 2Mhz crystal in conjunction with several gates of IC24, a 4049 CMOS oscillator chip. This clock generates CLOCK and a driving signal for a pair of one-shots. The one-shots (IC23 — no IC number was given on the schematic originally) comprise both halves of a F4123 and are used to generate 01 and 02 clock signals. This is not a bad way to produce these non-overlapping clock signals.

The variable oscillator utilizes the remaining sections of IC24 in a free-running oscillator whose frequency is controlled by a precision RC network, and the frequency may be varied by adjusting R33, a 20K 20 turn trimpot. The variable oscillator presents phase one and two to the bus. CLOCK is always a function of the crystal oscillator and is always maintained at 2MHz by that clock so that peripheral cards may be made to operate correctly regardless of processor speed. See the section on High-speed operation for details on this.

Regardless of which clock is selected, if the variable clock is tuned to within 100KHz or so of the crystal, there is a tendency for the 2 clocks to "lock in" to each other, that is to get into a fixed resonance. The operational effect of this is that when the variable clock is selected in this condition, initial frequency change either up or down will tend to be resisted until the frequency "jumps" roughly 50KHz, at which point smooth frequency adjustment may be made.

Two augat pins (in area "B" and "C" respectively on the board) are provided for observation of the phase one and phase two signals. These points are test points only and not intended for adjustment of clock speed. Clock speed should always be measured at point C in area A. (On my board area C was hard to find because of the loss of silk-screened information.)

By removing the jumper choosing either of the two

on-board clocks and connecting the common pin (C) to an external frequency source, the ZPU card may be synchronized with another system if the user chooses. This also makes it possible to run the processor at very low speeds (down to DC) which on occasion can be tremendously useful. (For example, individual T-states may be observed on the front panel.) This is one of the nice hardware features of the Z-80. It would facilitate matters if a coax connector could be placed at the top of the board to aid in bringing in this external clock.

A visual inspection of the ZPU card reveals more buffers (8T97s or 74367s, ICs 1 - 10) than are usually seen on a CPU card. This additional buffering was necessary to reduce bus loading and to assure normal front panel operation.

The front panels of both the Altair and the IMSAI look at the high order addresses for information about the I/O port number during I/O operations. This was optional with the original designers of the 8080 systems because the I/O port number is output to both the high and low order addresses by the 8080.

The Z-80 outputs I/O port information only to the low order addresses. (Contents of the accumulator are then present on the high order addresses.) Hence, in order for the sense switches to operate normally 8 additional buffers have been added which transfer the lower 8 bits to the high order address lines during I/O operations.

The normal configuration of the ZPU card is that which enables it to operate in an Altair or IMSAI with other peripheral boards.

The kit as supplied and the instructions as given result in a CPU card which may act as a direct replacement for your current 8080 processor. There are however some options which may be exercised by the user which take advantage of several of the Z-80 options. These are:

1. Connecting the REFRESH signal to pin 98 on the bus.
2. Connecting the non-maskable interrupt to vectored interrupt lines.
3. Altering the processor speed.
4. Use of the duplicate PRDY line.

Pin #28 of the Z-80 outputs a RFSH signal, which may be used to provide refresh timing for dynamic memories. This signal may be placed on pin #98 of the bus. Pin #98 is normally occupied by SSTACK on the S-100 bus 8080 system, however this status indicator is not terribly useful and was omitted on the Z-80 altogether.

The RFSH signal may be picked up at area F, immediately to the left of the Z-80, and "jumpered" to the pad in area G, straight down and slightly to the left from the Z-80. This places the signal on the bus.

When the signal is on the bus, the status light on the front panel, labeled STACK will now stay lit when the processor is running, indicating that the REFRESH signal is on the bus.

For the exact timing information about the RFSH signal, see the Z-80 manual. This signal is useful to systems utilizing dynamic RAM storage.

On the Z-80, pin 17 is NMI, the non-maskable interrupt. To quote the Z-80 manual:

"The non maskable interrupt request line has a higher priority than INT and is always recognized at the

end of the current instruction, independent of the status of the interrupt enable flip-flop. NMI automatically forces the Z-80 CPU to restart to location 0066_H.

This powerful interrupt capability is made available to the ZPU user.

Pin #17 of the Z-80 and pin #4 of the bus (VIO) are normally both held high by pullups. Solder pads at location H and location E may be jumpered together, thus making the NMI available at VIO, the highest priority vectored interrupt line.

The Z-80 has the capability of operating from DC on up to some maximum limit greater than 2.5MHz because of its static nature. To take full advantage of this capability the ZPU card has been designed with a variable speed clock on-board.

P #1, an augat pin soldered to a wire represents the phase one and two inputs to the processor. If the pin is placed in J2, the augat pin labeled "V" in area A, then by adjusting the trimpot located above the crystal, the frequency may be varied over a range of approximately 3 MHz.

Normally, when one is reducing the speeds, simply turning the speed down is sufficient, and no problems will be encountered. For individuals whose systems may currently be marginal at 2MHz, reducing the processor speed may well greatly increase reliability of the system. Some marginal memories may operate with no wait states if the clock is set at about 1.5 MHz.

When speed is increased it is sometimes necessary to readjust the timing of the 74123 for stable operation. This RC network (R36 and C26) effects the phase one and phase two relationships, which become more critical as processor speed is increased.

The duplicate PRDY line was included in order to facilitate operation with the Altair 8800B, or for any other use the user might dream up.

The extra PRDY line comes off of IC17, area D, immediately to the left of the IC has 2 pads which are normally **jumpered** together. If one wishes to use the extra PRDY line, remove the jumper, and take the PRDY signal off of pin #3, the top of the two pads.

The 8800B requires 2 additional RDY lines. XRDY2 is on bus line #12. If operation with the 8800B is desired, **jumper** the additional RDY line on the ZPU to this bus pin. The other RDY line is FRDY, which is pin #58 on the bus. The user may use this line as he wishes.

The Z-80 unlike the 8080 does not necessarily stop on an M1 state. In order to operate the front panel, the processor must, however, be in the M1 state. TDL has decided to omit additional circuitry which would force the Z-80 to halt at M1. Therefore when operating in single-step mode it is necessary to make sure that you step the processor to an M1 state and then operate the front panel.

The Z-80 chip itself is guaranteed to operate up to 2.5 MHz. Most Z-80's appear to operate in the neighborhood of 3MHz and some will operate at 4MHz. TDL has designed the ZPU board to operate reliably at clock speeds up to 4MHz. The ZPU manual contains an excellent section on high speed operation of the ZPU, including a simple procedure for adjusting the speed of the processor using the TDL SPU to its maximum.

It is important to note that although the system CLOCK line is maintained at 2 MHz regardless of processor speed, some boards use 01 or 02 for their

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timing. These boards will not operate correctly when the processor timing is altered. In order to fix this problem, simply cut the clock trace on the non-operating board (from 02 or 02 and *jumper* it to the CLOCK line.) I have done this routinely on all my I/O boards so that I may substitute either the ZPU or the CPU card at will.

The TDL ZPU manual contains a section on compatibility. Bear in mind the fact that there are two types of compatibility, hardware and software. In general, with the exception of the SSTACK signal and the previously mentioned single-step problem, hardware compatibility between the TDL ZPU and the S-100 CPU has been achieved. The front panel of your system will operate in its normal fashion with all switches serving their normal function.

The Z-80 is 100% machine code compatible with the 8080's seventy-eight instructions. Hence standard 8080 software will run without modification on the Z-80. However, if you are using software controlled timing by means of the number of machine cycles necessary to complete a loop, 100% compatibility will not exist. The problem is inherent in the Z-80. The architecture of the Z-80 is more efficient than that of the 8080. In its design many instructions of the 8080 - while having the same machine code, have fewer "T-states": thus the instruction is executed faster in real time.

Obviously where the real time length of a timing loop is controlled by software, the program will have to be rewritten to adjust for the higher realtime execution speed of the Z-80. This is true even if both the 8080 and the Z-80 are running at exactly 2MHz. In the

benchmark programs the Z-80 running only the 8080 instruction set has been found to be about 10% faster even while being maintained at 2MHz clock speed.

TDL notes that almost all 8080 languages run without a hitch on the TDL ZPU. The sole exception is Altair Basic. This Basic has as part of its routines several occasions where the parity flag is checked as part of the function. In the Z-80 the parity flag indicates OVERFLOW and not parity during math routines. As a result Altair Basic will not run on the Z-80. However, the structure of the Basic language does not require this use of the parity flag; it was used to reduce program space by several bytes. It therefore can be patched by those who wish to do so. An attractive alternative would be to procure TDL's 8K Basic which is Altair compatible and which contains a large number of exclusive and desirable features. Another solution would be to buy one of the Z-80 Basics now available which provide operational features. They are not, however, 8080 compatible.

The ease of assembly, low cost, and special features of the TDL ZPU make it a good alternative to the standard CPU card. In addition TDL's ZPU manual is very comprehensive and the Zilog Z-80 is also included. TDL also provides a listing and paper tape of their ZAP monitor.

The ZAP Monitor is a 1K version of TDL's 2K ZAPPLE Monitor. It is relocatable (can be placed anywhere in memory), expandable ("modules" of additional commands can be tacked on at the end, like cars on a freight train.), and quite powerful as a system executive.

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The expandable feature should be of great interest to the user. Since it is designed in a modular fashion, and since the ZAPPLE is its direct parent, this monitor features tremendous expandability - either of routines generated by the user, or by routines provided by Technical Design Labs. Several "modules" which will be of great interest include powerful "breakpoint", "search" and "register display" commands.

For only \$269.00 the TDL ZPU represents a very nice low cost means to enhance your S-100 bus system.

(16)

ZPU PARTS LIST

IC 1 to 10	8T97 or 74367
IC 11, 12, 20	74LS02
IC 13, 15, 19	74LS04
IC 14	74LS30
IC 16	74LS74
IC 17	74LS10
IC 18, 21, 22	74LS00
IC 23	74123
IC 24	4049
IC 25	Z-80
IC 26	7805
R 1 to 10	1K, 5%, Brown, Black, Red, Gold
R 12 to 20	1K, 5%, Brown, Black, Red, Gold
R 30	1K, 5%, Brown, Black, Red, Gold
R 11, 31	100 ohm, 5%, Brown, Black, Brown, Gold
R 21	47 ohm, 5%, Yellow, Violet, Black, Gold
R 22 to 29	4.7K, 5%, Yellow, Violet, Red, Gold
R 32	4.7K, 5% Yellow, Violet, Red, Gold
R 34	3.3K, 5%, Orange, Orange, Red, Gold
R 35	10K, 5%, Brown, Black, Orange, Gold
R 36	12K, 5%, Brown, Red, Orange, Gold
R 33	20K, 20 turn trimpot
C 1, 2, 14	47Mf, 25V, dipped tantalum electrolytic
C 3 to 13	.1Mf Disc Ceramic
C 16, 18, 19	.1Mf Disc Ceramic
C 15, 17	.001Mf Disc Ceramic
C20	33Mf, 25V dipped tantalum electrolytic
C 21, 24	.1Mf Disc Ceramic
C 27 to 31	.1Mf Disc Ceramic
C 22	10Pf Disc Ceramic
C 23	6 Pf Disc Ceramic
C 25	27 Pf Disc Ceramic
C 26	47 Pf Disc Ceramic

Y1	2Mhz Crystal
J1A	10 pin molex connector
J1B	16 pin high profile DIP socket
J3, 4, 5, 6	Augat pins
P1	Augat Pin
1 Heatsink	
1 ea. 6/32 x 5/16"	machine screw, lockwasher, nut
1 ZPU PC board	
12	14 pin low profile IC sockets
12	16 pin low profile IC sockets
1	40 pin high profile IC socket
Miscellaneous	
6"	jumper wire
5'	solder
1	Zilog Z80 CPU Technical Manual
1	ZPU Documentation Manual
1	Paper tape of the ZAP monitor

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COMPUTER COUPLING

By B. D. Lichtenwalner

With a little time and diligence you
can turn that old Boudot coded
teletype into a reasonable terminal
for home computing

Recently several articles reminded us that good old five level, Baudot coded, teletype machines could be used with a hobby computer. With only a few programming steps code conversion could be accomplished. Add a timing loop and the parallel characters from the computer bus could be serialized; but how about the interface to those printer magnets that require about 150 volts to operate effectively? Or how about all those hams that want to link their new computer to their terminal unit and get on the air with a buffered text system, an automated answer back system, or one of those really fancy mail box/replay systems? Here is a circuit that will allow linking teletype loops with open circuit voltages from 100 to 220 volts to your computer without any danger of getting high potential voltages onto the computer chassis. Also the noisy teletype grounds are not tied to the computer chassis. The circuit will provide both "1" and "0" level outputs for mark, and will accept both "1" and "0" level inputs for mark for keying the loop. Provision is also made to have the output blanked for inputs generated by the coupler circuitry.

Circuit Description

Two opto-isolators are used at the heart of the circuit to isolate the loop voltages from the TTL logic compatible interface to the computer. OP1 has the loop current flowing thru it, and as a result turns on the photo-transistor on the device. As a result the output voltage on pin [5] of the OP1 is low. With the output of OP1 low, the inverter, U1, provides a high level TTL output at circuit output pin [4]. (Boxed Numbers relate to the numbers used on the printed circuit board used in this configuration.) The next section of U1 again inverts the signal and provides the user with a "0" level signal when the loop is conducting. (circuit output pin [5]). When the loop "opens" as a result of keying, or receiving a signal, if tied to a terminal unit TU, the output at [4] will go low and the output of the circuit on pin [5] will go high. The delay components (C2 and R3) are used as part of the circuitry to defeat the receiving section from seeing the output from the transmitting section and will be explained later. R2 and the light emitting diode, LED, are used to indicate that the loop is drawing current. It will give the user an indication that the loop is operational, and will blink on and off when the loop keys. It is not necessary and may be omitted if you don't like all that flashing going on while operating.

TO TELETYPE LOOPS

The second iso-coupler, OP2, is used to key the loop (open the circuit). Transistor TL really does the job, and the isolator just provides power to the base to make sure it turns on when the loop should be closed. The circuit works like this: the light emitting diode in the opto-coupler, OP2, is turned on by the current drawn thru R5. This makes the phototransistor in the opto-coupler conduct. Full loop voltage is then applied to the base of the transistor with R9 as a current limiting resistor. When input pin [3] of the circuit is brought to ground the opto-coupler does not conduct, hence removing the forward bias of transistor, T1, and allowing it to turn off. When the transistor is off the loop current drops to the open circuit (Space) condition. It will not quite drop to zero since the circuit does steal a bit of power from the loop to operate. This minimum current is determined by the open loop voltage and the value of R9. The 33K value is great for loop open circuit voltages from 80 to 250 volts. (Range on your machine may drop some on the extreme ends of these voltage ranges.) If you run higher voltages, increase R9. If your loop has an open circuit voltage lower than 80 volts, decrease R9. I have used this circuit to key a 24 volt loop by reducing R9 to about 7.8K. (Use the highest value that produces good results.) If you want to drive the loop with a mark = "1", connect your input to pin [3]. If this is your input pin make sure that input pin [2] is grounded. If you let TTL logic float (open circuited) it will assume the input is in the "on" condition, and the output of U1, pin [4] will always have a "0" level on pin [1] of the opto-coupler. This will always make the loop run "open."

Just one more note about the circuit used in keying the loop. Zener diode D5, is used to prevent excessive voltages from appearing across the collector-emitter junction of OP2. Be sure not to let it out.

The diode bridge consisting of D1-D4 is added to make it convenient when connecting into a loop. I can never remember which polarity is which, so for a few cents I don't have to worry about it. R1 and C1 are transient voltage suppressors to keep out spikes when the loop is going from mark to space. Always a good investment if you are a conservative circuit designer.

Construction

The components used in the project are all available from companies that advertise in this magazine. The total cost of the project for components will be around \$10.00. The circuit is easy enough to lay out on

perf board, but I prefer to use printed circuits. A circuit board is available from Scott Communications for \$3.50. Whether you wire by hand, make your own board, or get the board from Scott the following notes should be helpful in building and getting your unit working. First, make sure the diodes are in the proper direction. If you buy surplus, as I do, it is worth the time to make sure the labeling is correct. A simple ohm meter check is enough. Be especially careful with the Zener. You won't hurt anything if you get it wrong, but your loop will run "open" all the time. Also, assure yourself that the LED is in the right direction; backwards will make the output circuit inoperative.

Testing/Operation

Connect your +5 Volt power supply to circuit pin [1] ground pin [7] to your chassis and power supply. Also for test purposes tie pin [2] to ground temporarily. Connect the loop to pins [8] and [9] and turn on the loop. The LED should glow and the loop should operate as always. If it is running open, check that the input pin to the OP2 (pin [1]) is about +1.5 volts. If it is, check R9 and check that D5 is in the right direction. When the loop is "marking" you can check the keying circuit by opening the ground lead at pin [1] or by shorting circuit pin [3] to ground. Both conditions should make the circuit run "open." When the loop opens, the LED should stop glowing. To check the output circuit, connect a voltmeter from ground to circuit pin [4]. With the loop activated, and the 5 volt power supply connected, there should be a logical "1" on pin [4]. When the loop is keyed (signal received by the TU or pressing a key on the TTY machine) the meter should swing toward zero. Ungrounding pin [2] should give a solid "0" on pin [4]. When circuit operation is verified as correct, move the test lead to pin [5]. With the loop activated, this pin will be at a logical "0," and will go positive when the loop is keyed. Again, ungrounding pin [2] should give you a logical "1" on pin [5].

For some operations it is desirable not to have the output circuit follow the input circuit. To disable the output circuit from signals introduced into the input circuit, connect a general purpose diode between pin [3] and pin [6]. The anode is connected to pin [3].

Conclusion

The circuit shown provides a simple but effective way to isolate high voltage TTY loops from normal TTL

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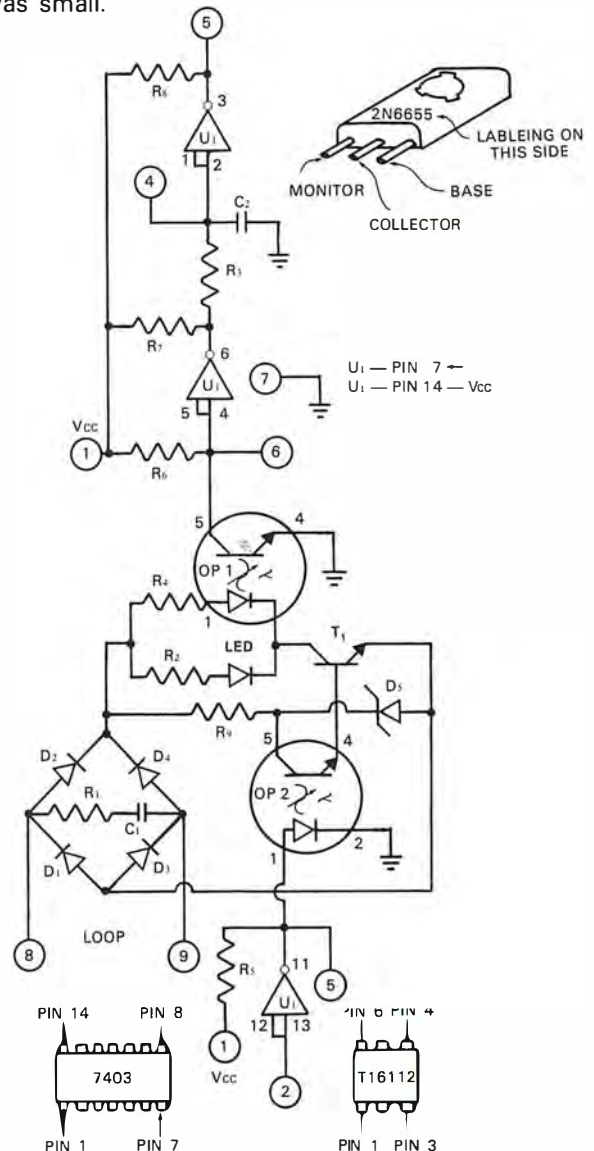
level circuits. It has the flexibility of being keyed by both polarity signals and also provides TTL level outputs with both a positive and negative signal for marking conditions. Commonly available parts and available circuit board makes this an inexpensive and easy-to-duplicate project.

Design Note

Values for R9 are calculated as follows

$$R9 = \frac{V_{OPEN\ LOOP}}{-3 + [R_{LOOP} \times 0.06]} \times 0.003$$

The original design was done for a loop with 100 volts open circuit and an assumption that the R LOOP was small.



PARTS LIST

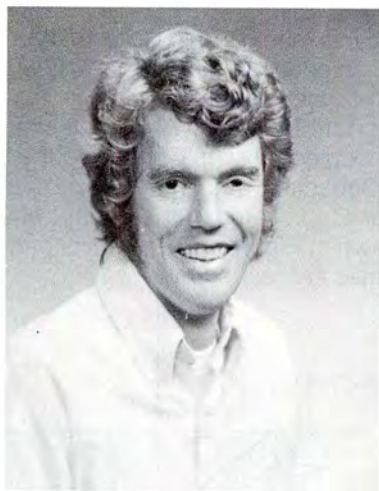
U1 — 7403
D1, D2, D3, D4 — IN 4005, 600 PIV,
1 AMP DIODE
D5 — IN 4732 — 4.7V, 1 WATT
ZENER DIODE
OP1, OP2 OPTO — COUPLER,
TI TIL 112
LED — SMALL RED LED
SIMILAR TO MVD 50
C1 — 0.1µf, 600V CAP
C2 — 0.01µf, 10V CAP
R1, R5 — 470ohms, ¼WATT R.S.
R2, R3 — 150ohms, ¼WATT R.S.

R4 — 47ohms, ¼WATT
R6, R7, R8 — 4.7K, ¼WATT
R9 — 33K, ¼WATT
T1 — 2N5655

○ INDICATES TERMINAL
CONNECTIONS FOR
CIRCUIT INPUT/OUTPUT

FIGURE 1

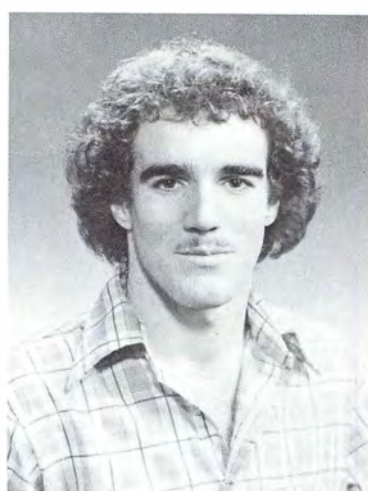
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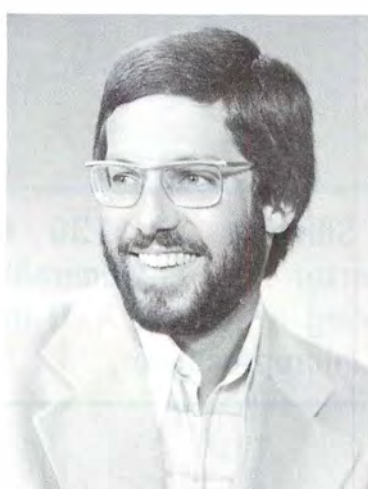
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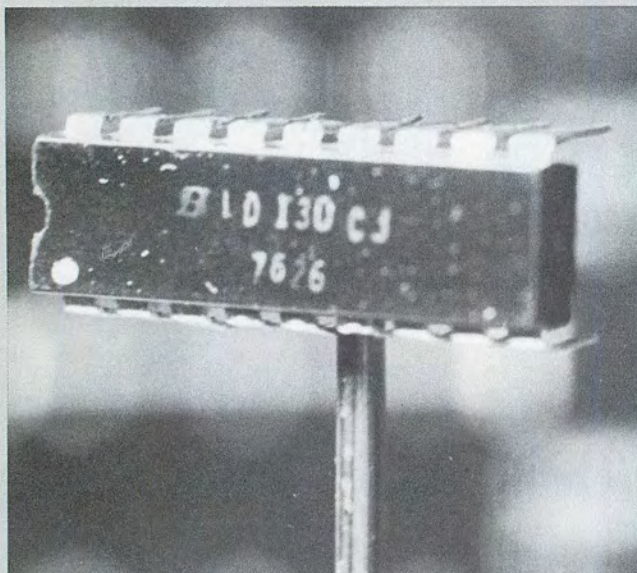
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The Siliconix LD 130 CMOS A/D Converter chip is admirably suited for providing a general A/D interface with your microprocessor.

We shall open this month's discussion of the LD130 by looking into the selection criteria for the external components and reference voltage.

Any sampling rate from 1 to 60 samples per second can be accommodated by simply changing the Integrator and Oscillator Capacitors (C_{INT} and C_{OSC}). To find the proper value for C_{OSC} , refer to the clock frequency vs C_{OSC} curve shown in Figure 1. The oscillator frequency and sampling rates are related by:

$$\text{Sampling Rate} = \frac{f_{OSC}}{6144}$$

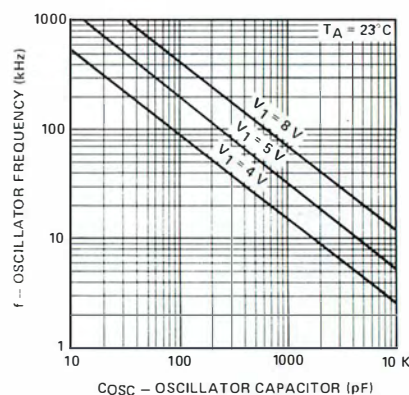


Figure 1. f_{OSC} vs C_{OSC}

In some applications it may be desirable to drive the OSC input with an external clock. This is a common requirement in many data acquisition systems. The LD130 can be driven by an external clock capable of going to logic high and low levels of $V_1 - 0.25$ V and 0.25 V respectively while sourcing or sinking 1 mA. This drive requirement is needed to override the drive capabilities of the CMOS oscillator input shown in Figure 2. A standard TTL gate will not be capable of providing this time requirement.

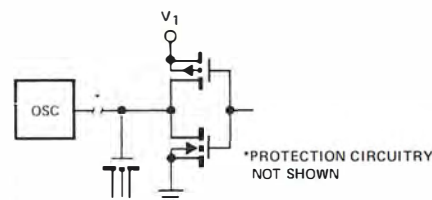


Figure 2. Oscillator Input

The integrator capacitor must change as a function of frequency by means of the following relationship:

$$C_{INT} \cong \frac{10^3}{f_{OSC}} \mu\text{F/sec}$$

THE LD130

Minimum supply voltages for operation are $V_1 = 4.3 \text{ V}$, $V_2 = -4.3 \text{ V}$. Although the LD130 will be functional at these voltages, TTL compatibility can no longer be guaranteed. Maximum voltages for functionality are $V_1 = 8 \text{ V}$, $V_2 = -8 \text{ V}$. V_1 and V_2 must be matched within 1.5 volts of each other or a zero offset will be created.

One of the major features offered by the CMOS LD130 is its very small power consumption (25 mW @ $\pm 5 \text{ V}$). This power consumption, however, increases significantly as V_1 and V_2 approach their maximum rated limits (60 mW @ $\pm 8 \text{ V}$). Low-power operation then dictates a lower supply voltage.

There exists a number of power supply and board layout problems that can lead to instability and poor performance in the LD130 A/D system. The problems arise from two main considerations— V_1 regulation and ground system layout.

V_1 regulation becomes important to the LD130 for a number of reasons. First, the LD130 linear stages are powered by the same positive voltage that supplies the logic section and, if used, a LED display. Display noise on this supply then must be rejected by the amplifiers. Since the LD130 has excellent power supply rejection for V_1 (0.6 mV change of output for a 1V change in V_1) this error source will be considered to be of secondary importance.

A major consideration is the modulation of the internal oscillator frequency by an unregulated V_1 . A glance at the C_{OSC} vs f_{OSC} curves of Figure 1 shows that this oscillator frequency is a strong function of V_1 . The V_1 seen by the LD130, however, can carry a considerable A.C. component when LED displays are used.

When interfacing with a microcomputer, the display problem does not exist. Proper attention should still be paid to grounding techniques to ensure that no logic currents are imposed on the LD130 ground return line. Furthermore the LD130 +5V supply should be well bypassed to ground and either a series diode or a regulator should be used to provide some series resistance on the capacitor filter. (See Figure 5)

The Auto-Zero capacitor (C_{AZ}) is not critical and should remain at 0.1Mfd over the full sampling rate range. In special cases of combinations of low sampling rates and high ambient temperatures (not usually found in home environments) a higher value may be necessary. Capacitor tolerance or type is not critical; standard ceramic disc types may be used.

Capacitors C_{AZ} and C_{INT} should be of a type which maintains a high insulation resistance over the temperature. All Film Type capacitors are suitable.

The equation
$$\text{COUNT} = \frac{V_{IN}}{V_{REF}}$$
 given last

month shows that a 2.000V reference is required to

By Roger Edelson, Hardware Editor

The "Quantized Feedback" conversion scheme introduced by Siliconix provides the LD 130 with AUTO-ZERO Auto-Polarity from a single reference voltage.

Part II of a Series

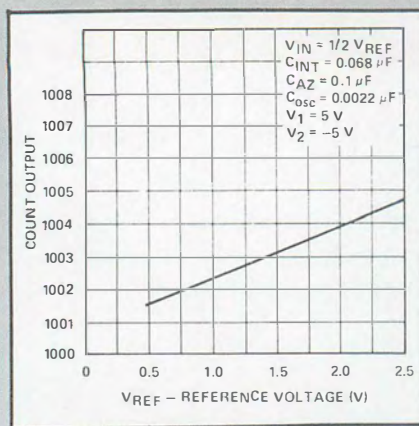


Figure 3. Ratio Operation

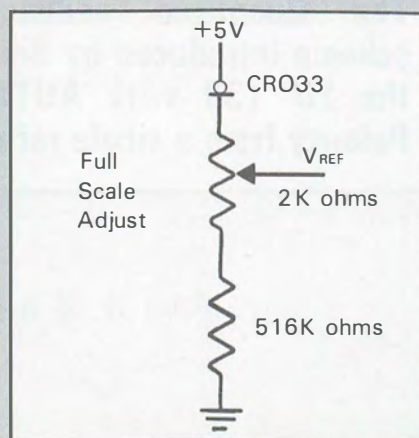


Figure 4.

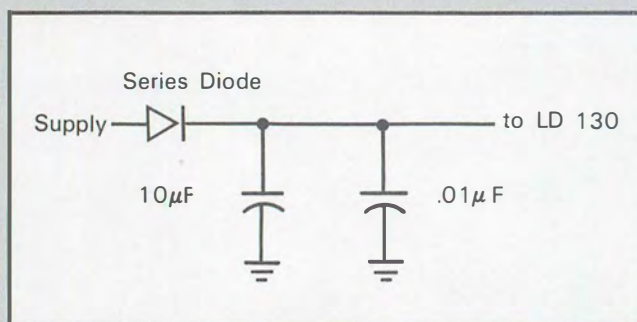


Figure 5.

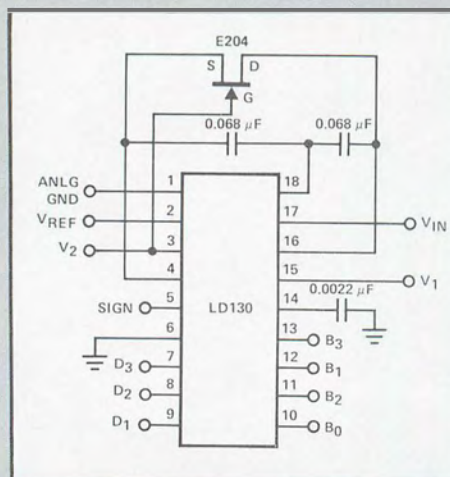


Figure 6. Lock-Up Protection FET

achieve an output that reads directly in millivolts of analog input (1.000 Volts Full-Scale). Scaling the output to read in other than volts can be achieved by adjusting V_{REF} according to this equation. It must be realized that the actual LD130 can vary by as much as 5% of the predicted values, so the V_{REF} must be adjustable for proper calibration.

Since the output of the LD130 is simply the ratio of the input voltage with the reference voltage, ratio measurements are natural to this system. The typical ratio operation error of the LD130 is depicted in Figure 3. A lower V_{REF} limit of 0.5V is recommended for a stable jitter-free output. Reference voltages less than 0.5 Volt provide an unstable reading due to the large amount of noise inherent in the CMOS op-amps.

The typical LD130 application as a 3 digit DVM shows the reference voltage being developed by a current regulator diode-resistor combination. (see Figure 4.) This is the preferred method for creating stable low-voltage references. The temperature compensated current regulator diode (the electrical dual of the temperature compensated Zener) keeps a constant current through the series connection of metal film resistor and cermet trimmer. A typical temperature coefficient of 50 ppM/ $^{\circ}C$ is achieved by this system—an order of magnitude improvement over a typical low-voltage Zener (IN746, 3.3 V Zener).

The LD130 specifications limit the maximum input current at V_{REF} or V_{IN} to 1ma. In order to prevent damage to the chip a current limiting resistor should be placed in series with these inputs if the voltage might exceed the supply voltage by more than 0.3V. A 250 K Ω resistor in series with pin #17 will offer input protection up to 250V over-voltage and accuracy would be degraded by only 0.025%.

The LD130 has protection circuitry at all inputs and output which prevent static damage by clamping the voltage at these pins.

The E204 JFET shown in the LD130 application of Figure 6 eliminates a power-on lock-up mode. This condition manifests itself by a constant 007 output. If the JFET is not used it may be necessary to recycle the power supplies to attain normal operation. The use of the E204 JFET reduces the maximum allowable negative supply voltage, V_2 to $-5.5 V$. A higher V_2 supply may be used if a higher pinch-off FET is used (E211 extends V_2 to $-6.5V$).

While both the Digit Strobe (D_1 , D_2 , and D_3) and Data Bit (B_0 , B_1 , B_2 , and B_3) outputs are capable of driving 1 TTL load, the maximum internal clock stability and thus A/D stability is attained when the bit outputs sink less than 400 μA . Therefore, CMOS or low-power Schottky TTL decoders are preferred. Standard TTL loads will not contribute to A/D instability when an external oscillator is used.

The interdigit blanking period allows the LD130 to interface with gas discharge displays when oscillator frequencies of 16 kHz or less are used.

Since the BCD data for each digit appears before and does not change until after the digit strobe (except when new data are loaded), interface problems such as latching of improper codes are minimized.

The net digit duty cycle is reduced to 25% by the interdigit blanking period. Average LED currents must be calculated with this consideration.

$$I_{AVG}(LED) = Z_{PEAK} \times 0.25$$

Since the total inter-digit blanking time is equal to a digit ON time, it may be used as a fourth digit strobe for special applications.

The ranging signals (overrange and underrange) are time multiplexed on the SIGN/UR/OR output. Demultiplexing consists of logically ANDING this output with either the D_1 or D_2 Digit Strobe output (see Figure 7). Thus:

$D_1 \bullet \text{SIGN/UR/OR} = \text{Underrange Pulse (active high) when count} < 80$

$D_2 \bullet \text{SIGN/UR/OR} = \text{Overrange Pulse (active high) when count} > 999$

$D_3 \bullet \text{SIGN/UR/OR} = \text{Plus polarity sign}$

If either an underrange or overrange condition exists, the appropriate pulse will occur once each sampling interval during the zeroing time. This single pulse can be used directly to step an Autoranging circuit into the next range. Figure 8 shows the implementation of an Autoranging System for the LD130.

The LD130 offers features useful in many data acquisition system applications. The compact size, low parts count, low power and BCD output of the LD130 can become important features in the trend to complex portable instrumentation. The integrating type "Quantized Feedback" conversion technique gives high noise rejection properties while offering conversion rates of up to 60 per second.

The fact that the LD130 offers mixed Measurement and Zero periods suggests that high rejection to specific noise frequencies can be obtained. While this is true, the rather variable nature of the LD130's internal oscillator makes it impractical to reject specific problem frequencies (such as the A.C. line frequency). An external oscillator can allow this maximum rejection (70 dB) to be attained by providing a more precise clock frequency. The proper oscillator frequency can be chosen from the following relationship:

$$f_{OSC} = \frac{2048 f_{noise}}{N}$$

where N is any integer that keeps the oscillator frequency within its prescribed limits (6kHz to 370 kHz).

The worst case Normal Mode Rejection for an untuned system is defined by:

$$\text{NMRR (worst case)} = -20 \log \frac{f_{OSC}}{4096 \pi f_{noise}}$$

The internal latches of the LD130 can be made to hold a reading indefinitely when a SPDT switch is added to the circuit as shown in Figure 9. In the convert position, the Auto-Zero Capacitor, C_{AZ} , is connected to the AZ input and the internal latches are updated after each conversion. When switched to "Hold", the large negative output of the AZ amplifier drives the Integrator to the positive rail. Since the comparator can never go low, the control logic retains the data from the conversion preceding the switch change to "Hold". While the "Hold" mode, the Auto-Zero function is inhibited. This means that V_{AZ} is no longer valid and that the first conversion after returning to the "convert" position will not be valid.

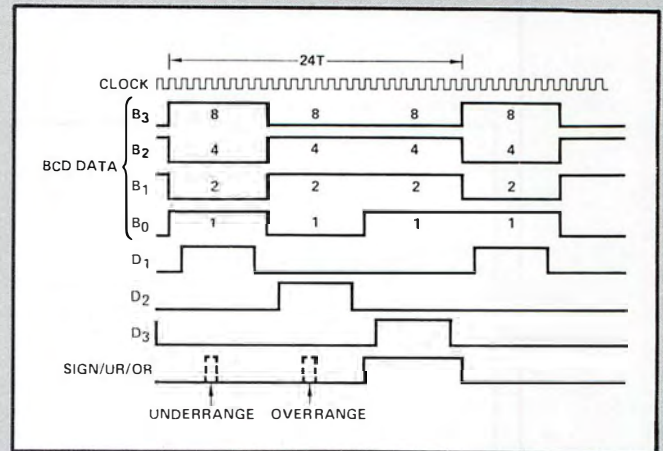


Figure 7. Data Output Format (Output = 769)

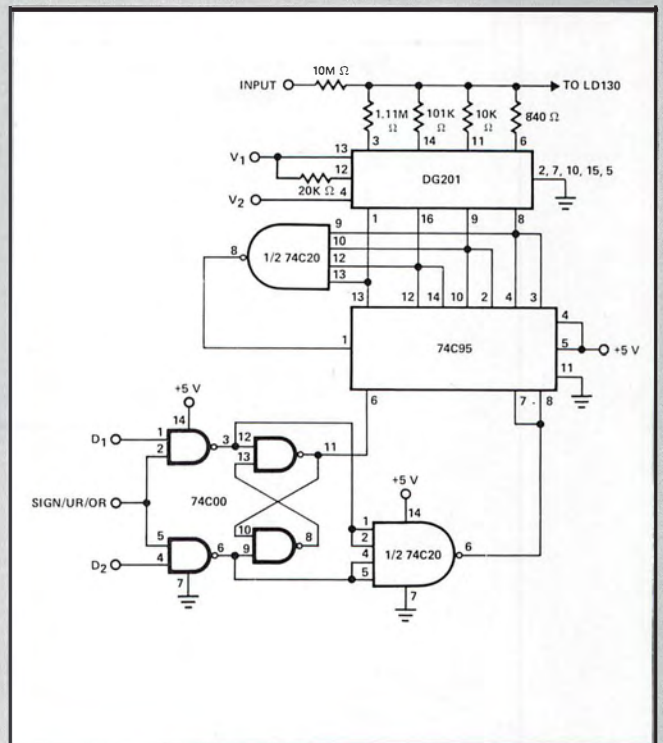


Figure 8. Autoranging System For LD130

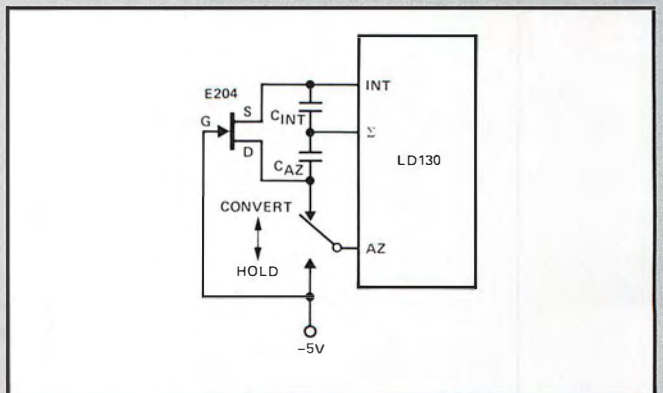


Figure 9. "Hold" Function

Note that the AZ line (pin #16) must be switched to $-5V$. Standard TTL logic can not be used in this case, but a SPDT analog switch operating from $\pm 5V$ supplies could be used. The Siliconix DG 300 series should provide this capability while allowing interfacing with standard TTL logic at its control pin.

Due to the limited number of pins available on the LD130, the internal system timing signals (M/Z, AZ) are not available to the outside. In the instances where A/D system timing may be needed, it may be decoded with the circuit of Figure 10. This circuit uses the integrator output (INT, Pin 4) to develop an End-Of-Conversion (EOC) signal that approximates the complement of the internal AZ signal depicted last month. The circuit can decode these states because the integrator operates around 0 volts during the Measurement and around -1 Volt during the Auto-Zero phase. The average value of the integrator then is indicative of the state of the AZ signal. The LD130 data are valid and remains valid as long as the output of the EOC circuit is "0". Switching of an analog multiplexer should occur during this time.

It is important, for the proper functioning of this circuit over the full analog voltage range, that C_{INT} be increased to twice the value given by Equation 2.

Although multiplexed BCD is more generally useful, the output of the LD130 can be demultiplexed and presented in a parallel format as shown in Figure 11.

Applications for this format include printer drive and interface to a 12 bit data bus. Interface to a printer would also require the presence of the End-Of-Conversion Signal as a Print enable. The EOC decode circuit is included in the schematic for this purpose. Multiplexed-to-Parallel BCD conversion is accomplished by the three CD4042 Quad latches. These CMOS ICs minimize parts count by eliminating the need for data bit buffers.

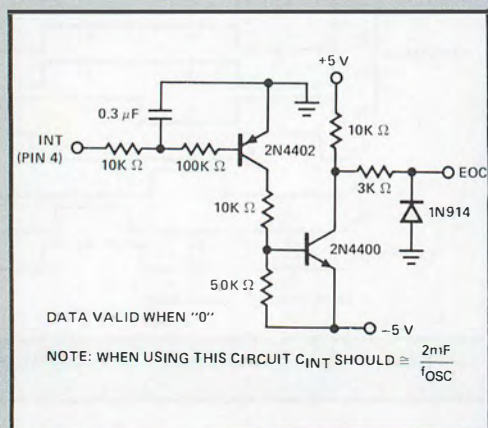


Figure 10. End-of-Conversion Decode

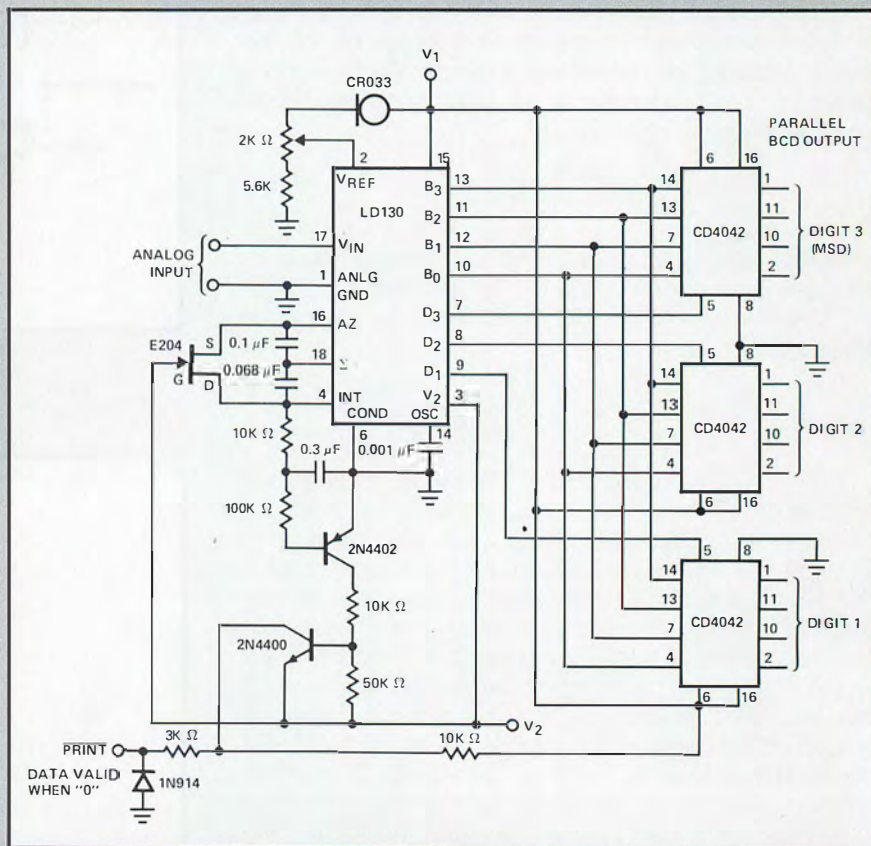


Figure 11. 3 Digit A/D with Parallel Output

The A/D- μ P system is the preferred method of handling and storing analog quantities. The cumulative errors of analog data handling are eliminated while powerful system functions can be achieved with a few ICs.

The LD130 A/D has many features important to μ P-based systems such as:

1. *BCD Coding* — The must useful format when the output is to be observed by humans.
2. *LSI* — Keeps system complexity down.
3. *Multiplexed Output* — Readily interfaces 4 and 8 bit systems.

One of the problems involved in interfacing the 4 bit μ P is that the 4 bit bus is fully taken up by the 4 BCD data bits. Additional bits for digit markers are not available. One solution would be to apply the digit strobes to an additional input port thus identifying the data. This method, shown in Figure 12, offers a simple hardware interface for the LD130 but requires an additional input port and a significant amount of processor time to synch up to the non-synchronized LD130. Here the circuit shown in Figure 10 is used to provide an end-of-conversion (EOC) signal to the μ P. The μ P must constantly monitor the input port containing this signal and use the information presented from D_3 , D_2 and D_1 to determine which digit is present.

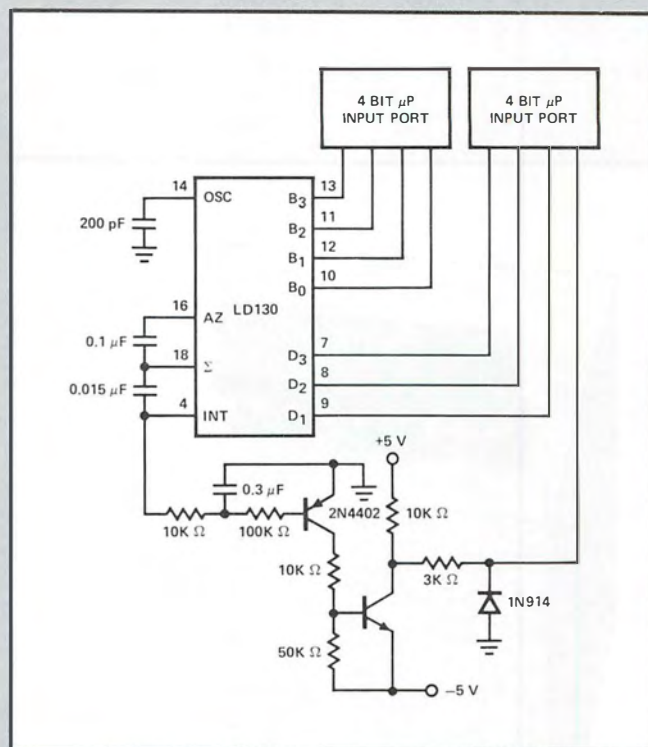
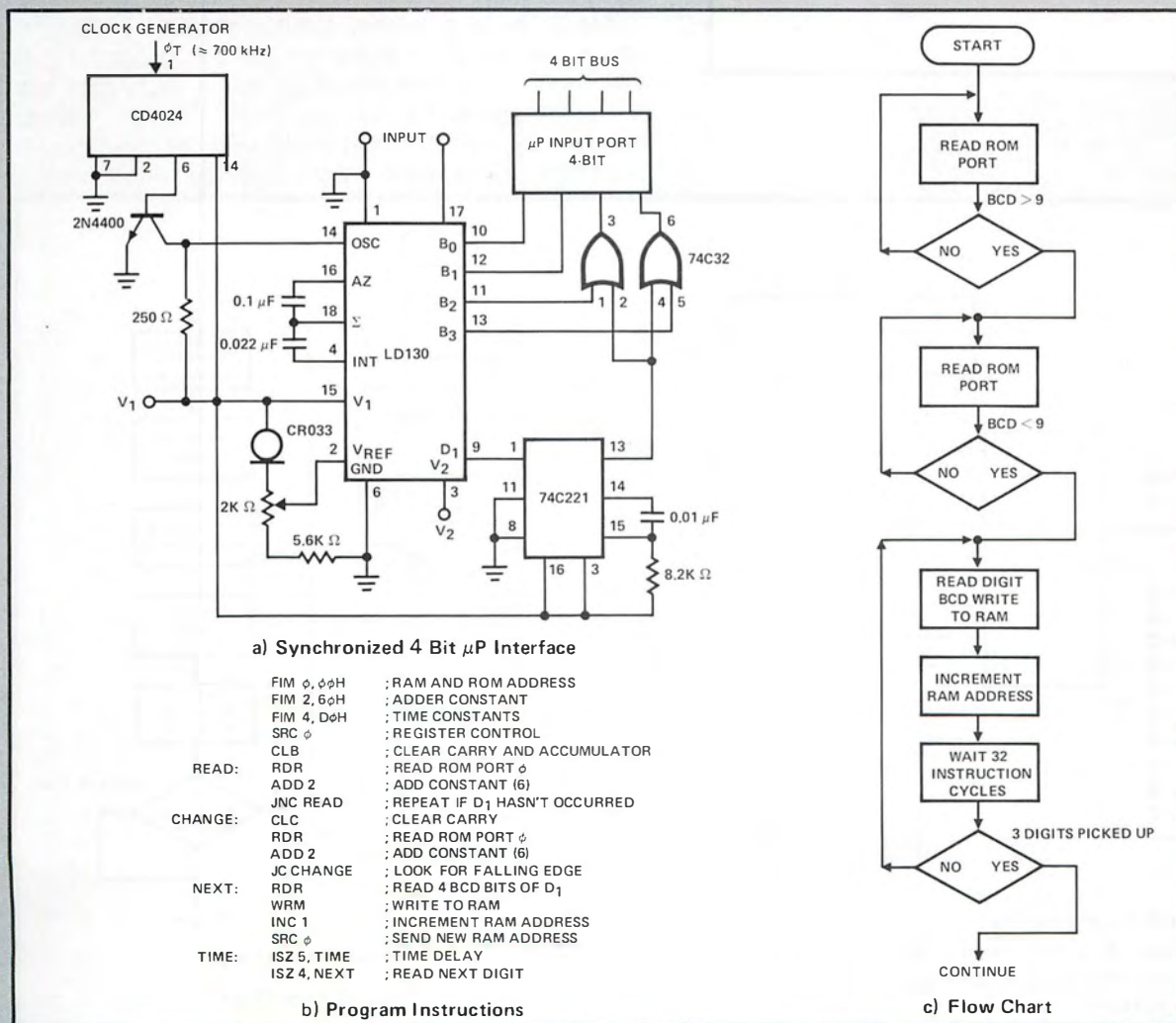
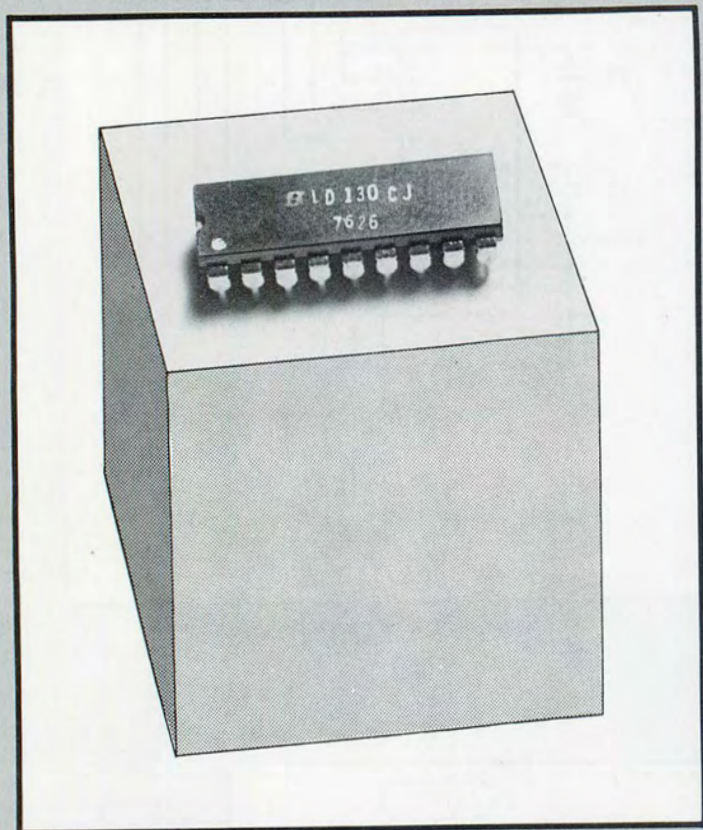


Figure 12. 4 Bit μ P Interface





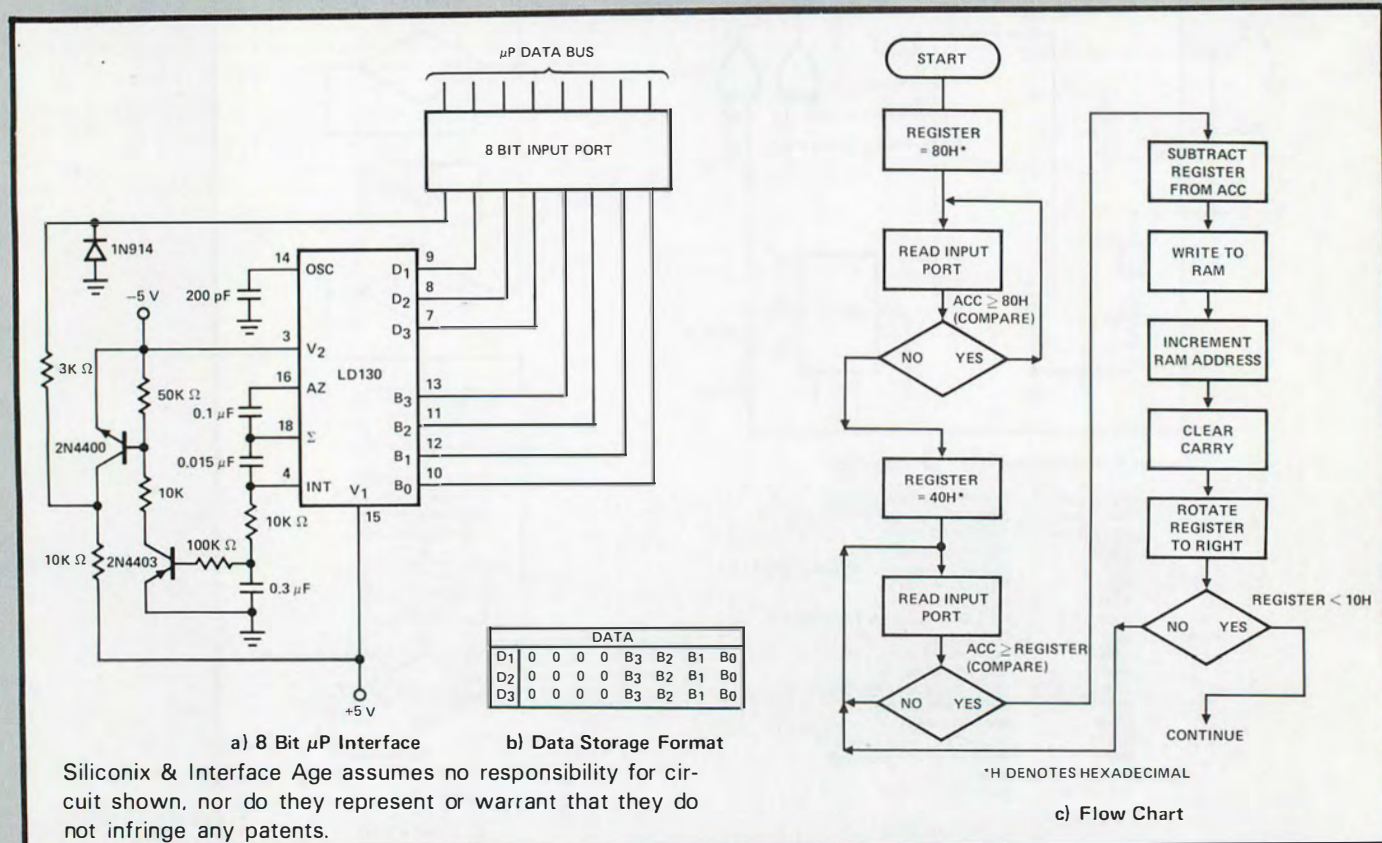
The interface shown in Figure 13 simplifies software and saves μP polling time by synchronizing the LD130 to the μP system clock. This application is designed specifically for the INTEL 4004, 4040 μP s. As shown in Figure 13a, the μP system clock is divided by 16 (by the CO4024 counter) before driving the OSC input of the LD130. The D_1 output of the LD130 triggers the one-shot which, in turn, forces an unallowed BCD state (11xx or $\geq C_n$) on the data bit lines—this is the cue that allows the μP to identify D_1 time. When the unallowed BCD state disappears, the μP picks up the D_1 data and stores it in memory. D_2 and D_3 data are picked up 32 and 64 μP machine cycles later respectively. Since the μP and the LD130 are synchronized by the common clock generator. The flow chart and software for this system are given in sections b and c of Figure 14.

Other counter types—74163 for example may also be used as may other one-shots (74123).

Obviously, the statement "3 Digits Picked Up" will have to be implemented by either incrementing or decrementing a register and checking the result. Maximum line-frequency rejection can be an added bonus of this system if the μP clock oscillator frequency is chosen to reject this specific noise frequency.

The interface shown in Figure 13 does not include the data valid (EOC) signal. This could be added to the system and the output logically "AND'ED" with the output of the one-shot. An alternative approach would be to simply repeat the pickup routine a second time to verify the data.

The 8 bit bus allows additional data markers to accompany the BCD data to the μP accumulator. Figure 14a shows all 8 lines taken up with 4 BCD data bits, 3 digit strobes and a data valid bit. This data interface requires the μP to occasionally poll the input port to determine if the data valid bit is low (input is less



than 80H). When this occurs, the μP then successively looks for the appearance of D_1 , D_2 , and D_3 by comparing with the numbers 40H, 20H, and 10 H stored in a working Register. Each of these numbers is consecutively subtracted from the data to yield the 3 digits of BCD data which are stored in memory (RAM) in the format shown in Figure 14b. These digits can then be combined into the desired format.

Some applications for the LD130 will now be discussed. A simple application of the ratio measurement feature of the LD130 would be as an angular or linear position measuring instrument. The linear potentiometer and two resistors, shown in Figure 15, are the only additional components needed for this measurement and serve both to provide the position to voltage conversion (0 to 100%) and the tracking reference voltage. Applying the voltage divisions from these resistors to the equation for COUNT

$$\text{Gives } V_{REF} = V_1 \frac{2R}{4R} = \frac{V_1}{2} \text{ and,}$$

$$V_{IN} = V_1 \frac{R}{4R} X \text{ where } X \text{ is the pot coefficient (ranging from 0 to 1)}$$

$$\text{then COUNT} = \frac{V_{IN}}{V_{REF}} (2000) = \frac{V_1 (R/4R) X}{V_1 (2R/4R)} 2000$$

which gives $\text{COUNT} = 1000X$

Scaling to degrees, centimeters, or any specific measurement unit simply involves solving for the appropriate divider resistors using the equation for COUNT.

A digital Thermometer, reading in either $^{\circ}\text{F}$ or 0.1°C , can be constructed by adding the circuit shown in Figure 23 to a basic LD130 DPM. This circuit converts temperature to a voltage by using the temperature dependent forward voltage of a PN junction as the sensing element. The change in this voltage is typically $-2.3 \text{ mV}/^{\circ}\text{C}$ at room temperature and can be suitable linear if the PN junction is biased with a constant current much greater than the reverse saturation current.

Since the diode will have a finite voltage at either a Celsius or Fahrenheit Zero, this voltage component must be subtracted out. Figure 16 shows the temperature sensing diode

(Base-Emitter of a 2N2222) biased with a 0 T.C. Current regulator diode (CR033). Zeroing is achieved by summing the currents from the CR033 and E506 diodes at the wiper of a potentiometer.

The scaling for either Celsius or Fahrenheit is achieved by adjusting V_{REF} according to equation for COUNT.

$$\text{Count} = 2000 \frac{V_{IN}}{V_{REF}}$$

$$\Delta \text{Count} = 2000 \frac{\Delta V_{IN}}{V_{REF}}$$

$$\text{for } \Delta T = 100^{\circ}\text{C} \quad \Delta V_{IN} \cong -230 \text{ mV}$$

$$\Delta T = 1000^{\circ}\text{F} \quad \Delta V_{IN} \cong -1.278 \text{ V}$$

Thus

$$V_{REF} = 0.46 \text{ V for } ^{\circ}\text{C} \\ = 2.5 \text{ V for } ^{\circ}\text{F}$$

The fact that the forward voltage decreases with temperature requires that the sense of the LD130 sign bit be inverted ("0" for +, "1" for -).

The LD130 offers substantial advantages in terms of cost, power, simplicity, and versatility to the A/D market. This chip offers simple interfacing the μP systems requiring few additional components and a simple software solution.

INTERFACE AGE thanks Gary Grandbois of Siliconix, the author of Application Note AN 76-5 "Applying the LD130" from which much of this material is derived. Further thanks go to Bryon McCullough, sales engineer for Siliconix who provided the application assistance without which the article could not have been written. Next month we shall cover a collection of I/Cs which should be of interest.

—R.H. Edelson

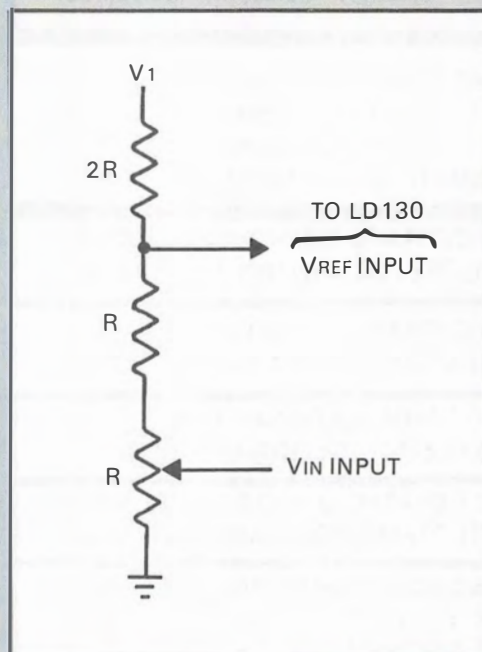


Figure 15.

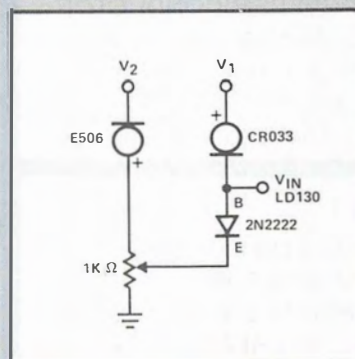


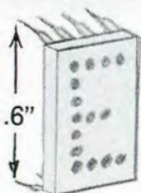
Figure 16. Temperature to Voltage Converter

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COMPUTER COMPONENTS

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1,024 BYTE EPROM
UV ERASEABLE
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\$1.00(1) 70¢ (10) 50¢ (100) 35¢ (1K)DB25's (S)\$3.00 (P)\$2.00 SHELLS \$1.00
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A COMPACT, POWERFUL COMPUTERPOLY I/O PROTOBOARD
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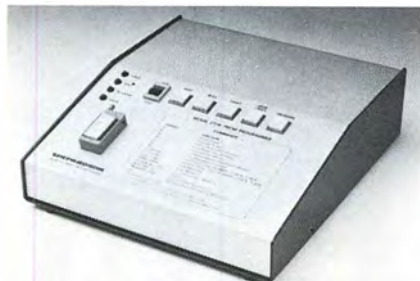
California Residents Add 6% Sales Tax

New Products

COMPONENTS

Low Cost PROM Programmer for 2704 & 2708 PROM's

Model 2708 PROM programmer, is an intelligent programmer that will program all major manufacturer's 2704 and 2708 PROM's.



The Model 2708 provides an RS232 and 20mA current loop interface as a standard feature. This allows the programmer to be used in conjunction with all printing and CRT type terminals, a paper tape reader/punch, or as a peripheral to the user's computer at baud rates up to 600.

The list price of \$850 makes it the lowest cost, highest performance programmer available. Because it has its own internal microprocessor, the Model 2708 provides many features and capabilities not available in other programmers.

1. Full editing capability allows the user to move, alter, and store data in the programmer's buffer memory in the user's choice of number base, binary, octal, decimal, or hexadecimal.
2. A printing terminal can provide the user with hard copy of the PROM data.
3. A paper tape reader can be used to input the desired data, and a paper tape can be generated to store the PROM data for later use and/or modification. The paper tape may be in BNPF, BHLF, binary, or ASCII hexadecimal format.
4. The programmer will automatically adapt to the terminal baud rate up to 600 baud.
5. The user can modify both the pulse width and the number of loops in programming a PROM, when used in conjunction with a terminal.

The versatility and low cost of the Shepardson Model 2708 make it a most attractive product to the user of 2704's and 2708's.

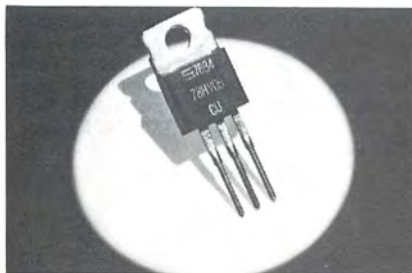
For further information contact R.C. Shepardson, Microsystems Inc., 20823 Stevens Creek Blvd., Bldg. C4-H, Cupertino, CA 95014; (408) 257-9900.

CIRCLE INQUIRY NO. 90

7800-Type Voltage Regulators from Signetics Feature Breakdown Rating Guaranteed to 60 Volts

An improved series of 7800-type high voltage regulators with a breakdown voltage rating 50% higher than competitive units is now available from Signetics.

The new devices, designated 78HV00, are 1 amp, three-terminal positive voltage regulators with a guaranteed input breakdown of 60 volts. The devices directly replace standard 40-volt versions of 7800 regulators. The higher rating can improve system reliability and permits larger transients and AC line fluctuations without system damage.



The 78HV00 units are the strongest 7800-type regulators available. With thermal shutdown and output transistor safe-area compensation incorporated in the monolithic package, they are virtually indestructible in standard circuit applications. Output current with adequate heat sinking is typically in excess of the specified 1 amp rating.

The 78HV00 regulators require no external components in fixed voltage regulator applications and offer internal thermal overload protection. Units in the line are available with output voltage ratings of 5, 6, 8, 12, 15, 18 and 24 volts in either TO-220 or TO-3 packages.

They are ideal for a wide range of applications, including local, on-card regulation for eliminating power distribution problems associated with single-point regulation. The 78HV00 devices can also be used with external components to obtain adjustable output voltages and currents, or as the power pass element in precision regulators.

Operating junction temperature ranges for the new units are available to -55 to +150 degrees C.

The 78HV00 high voltage regulators are available from stock through Signetics and its authorized distributors. As an example of pricing, 78HV05CU rated for 5 volts output in a TO-220 package is \$1.56 in quantities of 100-999; 78HV24CDA rated for 24 volts in a TO-3 package is \$2.26 in the same quantities.

For further information contact Signetics, 811 East Argue Avenue, Sunnyvale, CA 94086; (408) 739-7700.

CIRCLE INQUIRY NO. 91

Priority Encoders

Two eight-line-to-three-line low-power Schottky priority encoders are now available from Advanced Micro Devices.

The Am25LS148 performs priority decoding from eight inputs and provides a binary weighted code of the priority order of the inputs. This device is available in a 16-pin package and offers standard totem-pole outputs.

The Am25LS2513 is a gated three-state output version of the Am25LS148 in a 20-pin package. This device is particularly useful in the design of priority interrupt systems.

Both devices are available in molded and hermetic DIP and ceramic flat packages. Prices for the Am25LS148 start at \$1.94 in 100-piece lots.

For further information contact Advanced Micro Devices, Inc., 901 Thompson Place, Sunnyvale, CA 94086; (408) 732-2400.

CIRCLE INQUIRY NO. 92

Keyswitches

Build custom keyboards in minutes with the KBM series keyswitch. The model KBM is a low-cost, long life keyboard switch ideal for use in CRT terminals, data entry devices, hex keypads, touch tone encoders, etc. Semi-sealed construction means immunity to environmental contamination and the gold crosspoint contacts

insure reliable, low bounce switching for more than 10 million operations. Contacts are rated at 12 volts, 1ma, with less than 100 milliohms contact resistance. Mounting through an easily fabricated metal panel insures precise keycap alignment, and the rugged 1/16" terminals make hardwired prototypes a breeze.



A variety of keycap sizes, shapes, colors, and legends are available.

For further information contact George Risk Industries, Inc., GRI Plaza, Kimball, Nebraska 69145. Telephone (308) 235-4645. TWX 910-620-9040.

CIRCLE INQUIRY NO. 93

Smallest Coded DIP Switch

"MICRO-DIP," a ten position coded switch, occupies only one half of a 14-pin DIP socket and it can be mounted/connected directly to circuit boards by hand or flow soldering.



Switch settings can be made in either direction with a screwdriver. Numbers on top of switch indicate detent positions. MICRO-DIP can handle loads up to 100 milliamps at 5VDC and operate in a temperature range of -10° to +60°C.

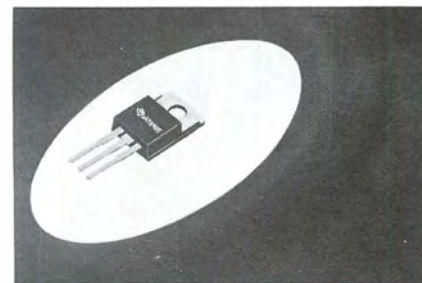
MICRO-DIP contacts are gold-plated. The .380" x .400" x .240" high glass filled epoxy housing provides a dust seal. Available codes include BCD complement, 1 or 2 pole 2 throw and 1-pole 5-position repeating in design. Priced under \$1.00 in 10K quantities; 6 week delivery for prototype units.

For further information contact EECO, 1441 East Chestnut Av., Santa Ana, CA 92701; Phone "Switch Products" (714) 835-6000.

CIRCLE INQUIRY NO. 94

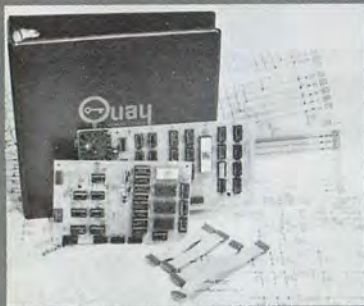
TI Regulators Keep Output Voltages Constant

Texas Instruments Incorporated has just sourced the very popular μ A78M and μ A79M series of fixed voltage regulators.



The μ A78M series are positive types, including those with nominal output voltages of 5V, 6V, 8V, 12V, 15V, 20V and 24V. They are

Microcomputer Quay 80AI does much more with the Z-80.



This dynamite new microcomputer system in a kit moves data like nothing else on the market. Run it alone or plug it into an S100 bus Altair/IMSAI. For solo performance, all you need is an unregulated power supply and an I/O device. Plugged in, Quay 80AI is a CPU, ROM, SIO, and RAM board—run any S100 compatible device. **BUT MORE THAN THAT.** Quay 80AI's Z-80 CPU opens challenging new areas of personal computing.

Features

- ☐ S100 bus compatible. Plugs in one slot of your Altair or IMSAI.
- ☐ Z-80 w/2.5 MHz clock.
- ☐ 1 K static RAM.
- ☐ 512 byte (ROM) monitor. Comes up running. Inspect, alter, dump, and load memory; set breakpoint; jump to user program. Handles serial I/O or keyboard input, including setting baud rate.
- ☐ 4 UVEPROM (2708) sockets.
- ☐ Serial I/O. RS-232 and 20 ma interface.
- ☐ Parallel keyboard input. Accepts standard ASCII keyboard.
- ☐ UVEPROM programmer. Program 2708 type UVEPROMs.
- ☐ 2 phase clock and sync. Run S100 compatible peripherals.
- ☐ 158 instructions. All 78 3080 instructions plus 80 new powerful instructions.
- ☐ On board voltage regulators.

Quay 80AI in a kit is \$450; factory assembled, \$600. Send for complete details. Or for fast action call 201-681-8700.

Mastercharge and BankAmericard accepted. COD with 1/3 deposit. N.J. residents add 5% sales tax. Price does not include shipping and handling.

Dealer inquiries invited.



P.O. Box 386, Freehold, NJ, 07728
Phone: 201-681-8700

available in the TO-220 KC package with an operating temperature range of 0°C. to 70°C.

The μ A79M series are negative types in the same voltage ranges. Both series are available in the TO-220 KC package and can deliver up to 500 milliamperes of output current.

The μ A78M and μ A79M series are interchangeable to the Fairchild series with the same designation.

Prices for 100 units are as follows: μ A78M series: \$1.09 each; μ A79M series: \$1.09 each.

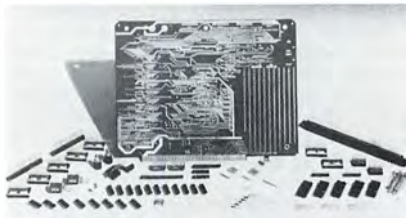
For further information contact Texas Instruments, Inc., Inquiry Answering Service, P.O. Box 5012, M/S 308, (Attn: Bulletin Nos. DL-S 7612403 and DL-S 7612405, June 1976), Dallas, TX 75222.

CIRCLE INQUIRY NO. 95

EQUIPMENT

UC 1800 Microcomputer

The UC 1800 is completely assembled and tested. As such, it has important design cost saving advantages to industrial users contemplating the use of microprocessors in their products.



The comprehensive instruction manual, simple straightforward software instructions, self-contained keyboard, and four digit hexadecimal display provide a package which promotes rapid training and system development.

All users will benefit from the growth potential incorporated in the UC 1800. External bus access allows future connection to a host of peripheral devices and add-on memory which can provide full mini-level computer power.

The user of the OEM version will find such features as full military temperature range, low power CMOS, single 3 to 15 volt supply and TTL compatibility are decided advantages in a wide range of product applications.

The outstanding features are: Low cost; Built-in keyboard programming; Digital (hexadecimal) display for address, memory contents, and I/O port; Front panel control of Interrupt, DMA, I/O Flag; 256 byte RAM expandable to 65.5 K bytes RAM or ROM externally; Low power consumption; Special circuit saves memory content when unit is turned off; Single power supply; Parallel and serial I/O data line capability; Available as single PC board microcomputer with or without on-board power supply for OEM applications.

The comprehensive documentation package of 230 + pages included with the UC 1800 provides extensive tutorial material with training aids on the theory and operation of digital computers. Both hardware and software are covered. Step by step instructions are given on programming. Programs for machine checkout and applications program examples are included.

Software included with the UC 1800 contains KEYBUG™, a keyboard handler and debug program which provides powerful software tools for generating and debugging your own programs.

A software library is available which contains diagnostics, useful macro building block routines, and games.

Option 001 — Automatically recharged internal battery. Allows program memory to operate

for up to four hours after power failure, \$22.50.

Option 002 — 120/230 VAC 50-500 Hz input power, specify which voltage is desired, \$15.00.

Also available in kit form, \$395.00.

For further information contact Infinite Incorporated, 1924 Waverly Place, Melbourne, FL 32901; (305) 724-1588.

CIRCLE INQUIRY NO. 96

Designer Evaluation Kit for Signetics 8X300 Bipolar Microprocessor

An evaluation kit that allows design engineers to evaluate the Signetics 8X300 bipolar microprocessor for planned applications is now available from Signetics.



The single-board evaluation kit includes all the elements a designer needs to judge the suitability of the 8X300 for system applications. The unit includes the 250-nanosecond bipolar microprocessor CPU, four input/output (I/O) ports for interfacing external devices, 256 bytes of working data storage. Programmable read only memory (PROM) devices in the kit are preprogrammed with input/output control logic, random access memory (RAM) control, and RAM diagnostic programs.

The microprocessor kit, designated 8X-300KT100SK, is intended to familiarize design engineers with the performance advantages of the 8X300, particularly for control and data movement applications.

The 8X300 features a 13-bit address bus for selecting instructions from program storage, and a separate input bus for entering 16-bit instruction words. With the 8X300, the entire process of data input, shifting, processing and output is accomplished in a single instruction cycle of 250 nanoseconds.

The board layout of the kit allows for variations and expansions of the basic design. All signals, for example, can be conveniently transferred off the board, and a wire-wrap area is provided for additions to the board circuitry. Additions may include memory, interfaces or special circuits for specific user requirements.

The 8X300 evaluation kits are available from stock through Signetics and its authorized distributors. Unit price of the kit is \$299.00.

For further information contact Signetics, 811 East Arques Ave., Sunnyvale, CA 94086; (404) 739-7700.

CIRCLE INQUIRY NO. 97

Communications Processor

The 40 Series Communications Processor is designed to perform such functions as data concentration, channel contention, message routing, polling control, speed and code conversion, protocol conversion, and voice response. The program is executed in nonvolatile Programmable Read Only Memory (PROM), and need not be "reloaded."



The basic system is self-contained on a single card Central Control Module, including a LED display and 10-position function switch for diagnostic test or system monitoring. Modular construction permits cost-effective single-channel or multi-channel configurations, with CPU, RAM buffer storage, PROM control firmware, synchronous and asynchronous communication interfaces, voice synthesizer channel modules and optional operator's console consisting of CRT and keypad.

Additional features include an Auto-Restart Timer and redundant common logic and power supplies for maximum reliability. The Voice Synthesizer produces clear, natural, male or female speech.

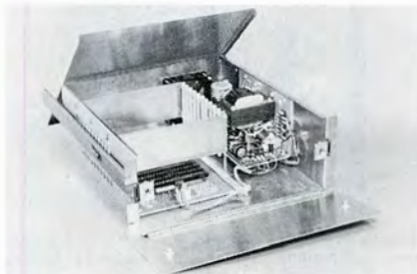
Normally supplied in turnkey communications controller systems complete with firmware, the 40 Series is also available to OEM's with a complete Program Development System to facilitate firmware development. Prices start at \$1800, with delivery of 45 days ARO.

For further information contact Roger Evans, Micom Systems Inc., 9551 Irondale Avenue, Chatsworth, CA 91311; (213) 882-6890, TWX 910-494-4910.

CIRCLE INQUIRY NO. 98

μC Hardware for the OEM

Supporting M6800-based equipment development, are chassis, card cages and a power supply for the MICROMODULE™ products. Two card cages are available; one with 5 card slots, the other with 10 card slots. Both card cages have mother boards that are pin compatible with the MICROMODULES and all of the EXORCISER modules.



The cages can be mounted on five different axes. The unit price of a 10-card cage is \$147.00; a 5-card cage sells for \$98.00.

For further information contact Motorola Semiconductor, Inc., P.O. Box 20912, Phoenix, AZ 85036; (602) 244-6900.

CIRCLE INQUIRY NO. 99

Control Store Sequencer Simplifies Bipolar Microprocessor Design

The random logic needed to implement microprogram sequencing in bipolar microprocessors can now be replaced by a new control store sequencer from Signetics. Designated 8X02, the new unit forms a powerful microprogrammed control section for computers, controllers or sequenced logic elements, when combined with standard Read Only Memory (ROM) or Programmable ROM (PROM).



The Signetics 8X02 is a low-power Schottky LSI device designed for use in high-performance microprogrammed systems. The basic function of the 8X02 is to control the fetch sequence of microinstructions. The unit is capable of addressing up to 1k words of microprogram, expandable to any microprogram size by conventional paging techniques. External page registers, when they are provided, can be controlled entirely or partially by the microprogram.

The 1k addressing capability is not available in other units, nor is the 8X02 subroutine nesting capability. The Signetics unit has a 1k addressing capability and a 8X02 subroutine nesting capability. A four-way stack register file and offers conditional nesting for branching to a subroutine or for automatic interrupt handling.

The 8X02 is easy to use, requiring just three control lines for the three-bit command code, versus from 9 to 18 lines for alternate units. Control instructions include Increment, Test and Skip, and Conditional branch to subroutine. The 8X02 uses a popular 28-pin plastic package.

The low-power Schottky process employed for the sequencer features good performance for both medium-scale computer applications and controllers. Chief applications are expected to be in central processing units (chiefly mini-computers); peripheral controllers such as high speed magnetic disc storage units, floppy discs and tape drives; vector generators for all types of CRT display terminals; and simple step controllers of various kinds. The 8X02 can be used for any system, however, that requires sequencing of instructions.

Cycle time for the 8X02 is 80 nanoseconds. The unit operates with a +5-volt power source with power consumption of 1000 milliwatts. The unit is totally compatible with all bipolar TTL logic elements.

The control sequencer architecture is shown in the schematic. The address register consists of ten D-type edge-triggered flip flops with a common clock. The address register can be loaded with different address sources under control of the three address control lines and one test input line.

The four-register stack input line with a two-bit stack pointer respond automatically to operations requiring a PUSH (write to stack register file) or POP (read stack register file). The file is organized as a four-word-by-ten bit matrix and operates on a last in first out basis. The stack pointer operates as an up/down counter.

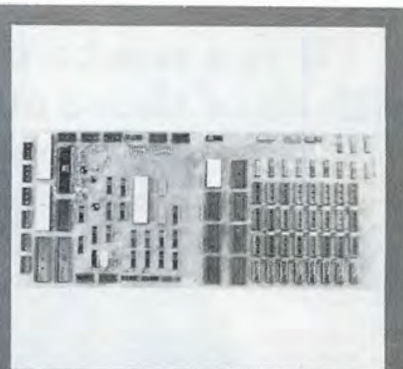
The N8X02XL Control Store Sequencer is available from stock through Signetics and its authorized distributors. Pricing is about \$19.45 in 100 quantities.

For further information contact Signetics, 811 East Arques Avenue, Sunnyvale, CA 94086; (408) 739-7700.

CIRCLE INQUIRY NO. 100

Datasc 1000 Computer, Controller and Tutorial Card

The Datasc 1000 card is available in two configurations: tutorial and populated. The tutorial has the following features: The MOS Technology 6502 microprocessor chip; one page of RAM (256 bytes); one-bit output latch; 8 data, 8 address and 9 control touch pads (our method of entering data with elegance and simplicity); 8 data and 8 address LEDs; single-cycle operation.



Microprocessor Quay 80MPS. For serious hobbyists.

Quay 80MPS is not designed for the casual hobbyist. Only if you're serious about your personal computing, should you find out about Quay 80MPS's features, capabilities, and options. Only if you want to break free from hobby-class microprocessors and enter a great new world of sophisticated computing experiences, should you get into the Quay 80MPS.

Features

- ☐ Single PC board, 16 pin dip connectors (no costly backplane or edge connectors.)
- ☐ Z-80 CPU, 158 instructions, 2.5MHz clock.
- ☐ 4K dynamic RAM. Expands to 16K on board (Z-80 refreshes w/o loss of thru-put).
- ☐ 1K UVEPROM monitor. Inspect, alter, dump, and load memory; set breakpoints; trace and single-step debugging; handles serial I/O.
- ☐ 7 additional UVEPROM sockets.
- ☐ 4 8-bit parallel I/O ports. Vectored interrupt (2 Z-80 PIO's, expands to 4).
- ☐ 1 socket for Z-80 4 channel counter timer.
- ☐ 1 UART. RS232 & 20 ma interface.
- ☐ UVEPROM programmer (2708).
- ☐ Fully buffered address, data and control.

Quay 80MPS is \$695, assembled and tested. Send for complete details. Or for fast action, Call 201-681-8700.

Mastercharge and BankAmericard accepted. COD with 1/3 deposit. N.J. residents add 5% sales tax. Price does not include shipping and handling.

Dealer inquiries invited.

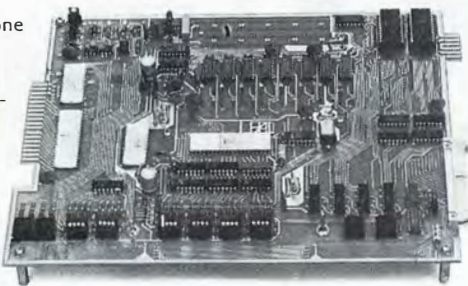


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Phone: 201-681-8700

CIRCLE INQUIRY NO. 27

If you want a microcomputer with all of these standard features...

- 8080 MPU (The one with growing software support)
- 1024 Byte ROM (With maximum capacity of 4K Bytes)
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- TTY Serial I/O
- EIA Serial I/O
- 3 parallel I/O's
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- Monitor having load, dump, display, insert and go functions



- Complete with card connectors
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- Completely factory assembled and tested—not a kit
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interface, power supply, ROM programmer and attractive cabinetry... plus more options to follow. **The HAL MCEM-8080. \$375**

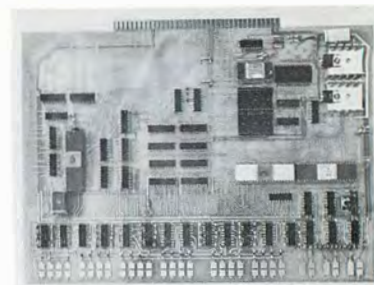
...then let us send you our card.

HAL Communications Corp. has been a leader in digital communications for over half a decade. The MCEM-8080 microcomputer shows just how far this leadership has taken us... and how far it can take you in your applications. That's why we'd like to send you our card—one PC board that we feel is the best-valued, most complete

microcomputer you can buy. For details on the MCEM-8080, write today. We'll also include comprehensive information on the HAL DS-3000 KSR microprocessor-based terminal, the terminal that gives you multi-code compatibility, flexibility for future changes, editing, and a convenient, large video display format.



HAL Communications Corp.
Box 365, 807 E. Green Street, Urbana, Illinois 61801
Telephone (217) 367-7373



In the fully populated form the Datic 1000 is a computer with the following features: full 16-bit addressing; total of 1K bytes of RAM (8x-2111); sockets for 2K of UV ROM (2x2708) for use as a dedicated controller; MOS Technology 6530-004 teletype I/O monitor (in ROM) plus 64 bytes of RAM plus 8-bit I/O port; complete interface to teletype current loop or EIA RS 232; high-speed cassette interface using the MC6850 ACIA, for storing programs; 6820/6520 PIA providing two 8-bit parallel I/O ports; fully buffered tri-state busses; power-on reset or restart; on-board address decoding for expansion; ribbon connector for I/O and edge connector for expansion.

The board is designed with capability for full expansion as described above, and for populating to a lesser degree for use as a controller. The Datic 1000 E fully populated card (less EROM) is available assembled and tested with power supply and a manual in single quantities for \$345.00. Availability is stock to 60 days.

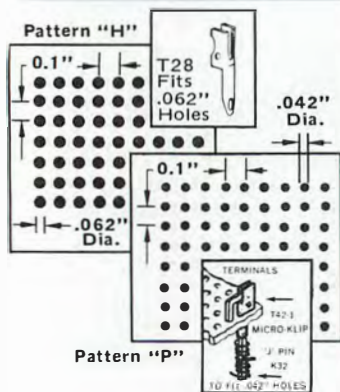
For further information contact DATAC Engineering, P.O. Box 406, Southampton, PA 18966; (609) 854-7852.

CIRCLE INQUIRY NO. 101

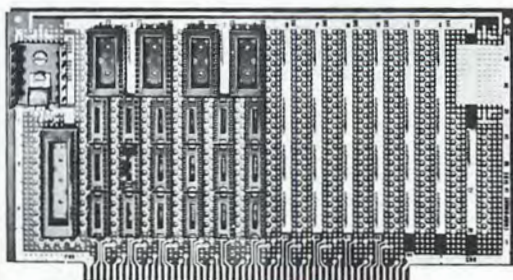
VECTORBORD® TENTH/TENTH HOLES MOUNT:

*DIPS, SIPS, KLIPS, CHIPS
 PINS, POSTS, POTS, PADS
 RCs, ICs, PCs, SCs*

Save Work — Time — Money



8800V MICROPROCESSOR PLUGBORD



(Component Side with Added Sockets)

Has 100 contacts on 0.1" centers, is 10" wide by 5.313" high. Has heavy tinned back-to-back buses, overall 0.1" spaced 0.042" hole pattern. Socketed models available.

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MICRO-VECTORBORD® "P" — 0.042" holes match DIP leads. Epoxy glass, or glass composite, paper, copper clad. Also 1/64" to 1/16" thick and 10" max. width.

VECTORBORD "H" — For larger terminals, leads. Available in epoxy glass sheets 4.8" to 8.5" wide and 8.5" to 17" long. 1/32" and 1/16" thick.

TERMINALS — Complete selection of wire wrappable and solderable push-in terminals for 0.042" and 0.062" dia. holes — plus wiring tools available.

PLUGBORDS — For solder or wrap wire construction 2.73" to 10" wide and 4.5" to 9.6" long. With holes .1"x .1", .1"x .2", .2"x .2", or loaded with IC sockets.

Precision Forty-Channel CB/RF Generator Achieves Crystal Accuracy in Low-Cost Unit

The RF Generator designated the Model 256 for 40 channel CB transceiver service incor-



porates features of particular benefit to CB service technicians. Five-band frequency tuning covers channels 1 through 40 on an expanded tuning range for easy, precise channel selection. Frequencies of 100 kHz through 16 MHz are covered on the other four bands to provide all IF requirements including: 455 kHz, 10.7 MHz, and any other, current or future.

Precision frequency selection is accomplished by connecting the counter output jack to a frequency counter for continuous monitoring. By use of the counter output in conjunction with a frequency counter crystal-controlled accuracy is available without the usual high cost.

A calibrated/attenuated output control provides RF signal output of 100,000 μ V down to less than 1 μ V for receiver sensitivity checks. The attenuated output is variable in 20 dB steps and by a 20 dB continuously-variable control calibrated in microvolts.

Internal modulation at a frequency of 1 kHz is variable from 0 to 100%, calibrated at 30%. Provision is also made for use of external modulation at frequencies from 20 Hz to 10 kHz through front-panel out/in jacks. When the Audio Output function is selected a 1 kHz audio signal

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is available at these same front-panel out/in jacks.

The Hickok Model 256 CB/RF Generator is available through Hickok distributors. Suggested retail price is \$199.00.

For further information contact Marketing Services Department, Hickok Electrical Instrument Company, 10514 Dupont Avenue, Cleveland, Ohio 44108.

CIRCLE INQUIRY NO. 102

Teletype Mobil Cart

The TTS Cart attachment adds mobility to any Teletype terminal. It is affixed to or removed from any Teletype in 30 seconds. It offers hand truck-like leverage and easy movement over door jams, carpet edges or even stairways. When the terminal and stand are in the upright operating position the wheels remain suspended above the floor to insure fixed installation stability.



The mobilized terminal may be rolled to any desirable location with ease.

Made of cold-drawn 1" steel tubing, high-tensile steel alloy spring clamps, 8" x 1 1/2" ball-bearing wheels. Size: height 38"; width 32". Weight: 12 pounds. Single unit price: \$59.50.

For further information contact TTS, 2928 Nebraska Ave., Santa Monica, CA 90404; (213) 829-2611.

CIRCLE INQUIRY NO. 103

Electronic 'Game-Playing' Organ

A computer-driven electronic organ that either plays your favorite song or teaches you how to play it has been developed.



The organ is one of three electronic "game-playing" devices that can be operated simultaneously by a single computer — in this case, a Computer Automation millicomputer, one of the smallest on the market.

The organ is controlled by a Computer Automation NAKED MILLI LSI-3/05, a compact, general-purpose machine priced as low as \$395.

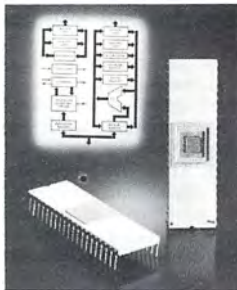
In the case of the organ-player, the NAKED MILLI is literally easy enough for a child to operate. For example, in order to learn how to play a particular song, the operator presses a start button and lights are illuminated over the organ keys to be pressed, in timed sequence. An automatic recording and playback feature enables the user to hear the notes he has played. He also has the option of simply playing any of the pre-recorded selections by pressing the appropriate button.

For further information contact Computer Automation, 18651 Von Karman, Irvine, CA 92713; (714) 833-8830; TWX 910-595-1767

CIRCLE INQUIRY NO. 104

"SC/MP-II" Microprocessor — Higher Speed, Lower Power Consumption, Single Voltage Source

Samples are now available of a new N-channel MOS version of the "SC/MP" 8-bit single-chip microprocessor that is twice as fast and which uses only one-fourth as much power as the P-channel version.



The "SC/MP-II" microprocessor has all of the features of the older version while offering several advantages over the P-channel device.

Power consumption of "SC/MP-II" is less than 200 milliwatts, considerably lower than the approximately 800 milliwatts consumed by the earlier version and the lowest power consumption of any N-channel MOS processor on the market today. Another significant improvement is that they have eliminated the need for two power sources. The "SC/MP-II" chip needs only a single source of +5 volts for operation, which is a great improvement over the first model which required two power sources — a +5 volt and a -7 volt supply.

The speed of "SC/MP-II" is twice that of the P-channel model. The new version takes one microsecond to complete a microcycle, and typical instruction execution time is 5 micro-seconds.

The "SC/MP-II" is fully compatible with its predecessor in terms of pin configuration, object code, and software, and with slight modifications to the crystal frequencies, it will be compatible with all of the "SC/MP" support equipment, such as the "SC/MP KIT" in the U.S.A., the "SC/MP INTROKIT" in Europe, the "SC/MP LCDS" (Low-Cost Development System), and the "SC/MP Keyboard Kit" which eliminates the need for a teletype machine.

The clock oscillator, which is located on the "SC/MP-II" chip, is designed to use very inexpensive television-type crystals of 3.58 or 4.0 megahertz. As an alternative to a crystal, the user may drive the clock with a standard TTL (transistor-transistor logic) timing system. In addition to the clock, all of the inputs and outputs are compatible with TTL devices and can also be easily interfaced with MOS and CMOS circuitry.

Sample quantities of the "SC/MP-II" microprocessor are immediately available from the factory. The price for a single sample is \$17.76, and production quantities of more than 2,000 will sell for approximately the same prices as the P-channel "SC/MP." Prices will be considerably lower in 1977 because we will then be able to offer the "SC/MP-II" in a plastic package.

For further information contact National Semiconductor, 2900 Semiconductor Drive, Santa Clara, CA 95051; (408) 737-5000, TWX 910-339-9240.

CIRCLE INQUIRY NO. 105

Quad OP-AMP Flip-chip

The popular MC3503 type quad operational amplifier is now available in flip-chip form as well as in conventional chip form and a variety of plastic and hermetic packages. The flip-chip consists of a silicon chip with solder bumps (90-10 solder on a chrome-copper-gold base) on the geometry surface to provide easy mechanical mounting and electrical connection.

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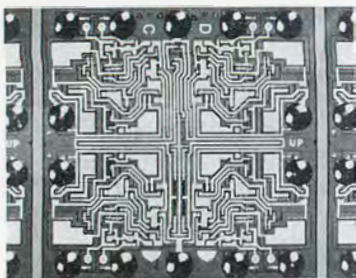
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CIRCLE INQUIRY NO. 42



Electrically the MCCF3503/3403/3303 offer much better amplifier matching than four single operational amplifiers. Each amplifier has characteristics similar to that of the MC1741 and in addition is designed with a Class AB output stage which minimizes cross-over distortion.

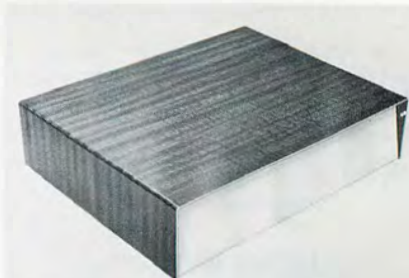
The flip-chip is offered at the following prices (in quantities of 100-900). MCCF3303 (-40°C to +85°C) \$2.25; MCCF3403 (0 to 70°C) \$2.50; MCCF3503 (-55°C to +125°C) \$6.75.

For further information contact Linear Marketing (602) 962-2122 or the Technical Information Center, Motorola Semiconductor Products, Inc., Box 20294, Phoenix, Arizona 85036.

CIRCLE INQUIRY NO. 106

Cases Enhance Custom-Designed Instruments

This line of economical enclosures, in two sizes and numerous attractive colors and finishes, gives desk-top instruments an appearance contemporary with sophisticated electronic components and systems. Designated Cono-Cases by Vector Electronic Company, the WA series enclosures incorporate a ten-degree sloped front panel and an optional smoked-plastic facing for behind-panel indicators. A recessed rear panel protects input/output connectors.



The enclosures, assembled from two interlinked channels, allow easy access to circuits, accessories and wiring. The lower section forms a chassis integrated with front and rear panels. Elongated holes in the bottom and rear panel provide superior convection cooling. The upper section serves as top and side panels. The WA1 enclosures are 11 inches wide by 8 inches deep by 4 inches high, giving 307 cubic inches of circuit space.

The WA2 enclosures are 14 inches wide by 11 inches deep by 4 inches high, providing a 560 cubic inch working volume. Construction of 0.062 inch (14 gauge) aluminum insures adequate support for transformers, heat sinks and other heavy components.

Cono-Cases are available with clear anodize satin finish, or with blue or walnut grained vinyl on the cover. Other colors available in anodize, vinyl or paint on request.

The WA Series enclosures are priced from \$12.95 to \$19.70, depending on model and finish. They are available off-the-shelf from Vector and will be available through the firm's distributors throughout the United States and Canada.

For further information contact Vector Electronic Company, 12460 Gladstone Ave., Sylmar, CA 91342; (213) 365-9661; TWX (910) 496-1539.

CIRCLE INQUIRY NO. 107

Low Cost Logic State Analyzer

A logic state analyzer, priced at \$272, including shipping and handling, places data domain analysis within the reach of smaller companies, educational institutions and hobbyists who previously could not afford the luxury of this useful development and troubleshooting technique.



The instrument, dubbed the Model 100A, is designed to operate with an ordinary oscilloscope and incorporates many of the features found on much more expensive analyzers including: a 16-word truth table display of ONE's and ZERO's; eight input channels with eight corresponding trigger word switches which can individually be set to "1," "0," or "X" (don't care); an internal data memory for post-trigger data collection; hexadecimal and octal formats; and both static and dynamic display presentations. These features permit the Model 100A to be used in typical logic state analysis applications such as tracing computer program flow, examining the contents of ROMs and other memories, checking counter and register operations, observing I/O sequences, and monitoring micromemory address steps.

The Model 100A can be used directly with a variety of logic families including TTL, Schottky, MOS, CMOS, and DTL. Connection to the

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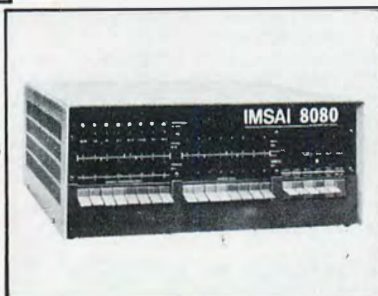
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The instrument comes with a 100-page manual which includes the theory of operation of the unit and the analysis procedures for seven common microprocessors. Also included are sections describing production testing, field service, and educational applications. Delivery is stock to 30 days.

For further information contact Paratronics, Inc., 150 Tait Avenue, Los Gatos, CA, 95030; (408) 354-7766.

CIRCLE INQUIRY NO. 108

Math Book Bonus with Purchase of Calculator

Anyone who purchases a TI-30 calculator soon will receive a free bonus — a 200-page book entitled "The Great International Math on Keys Book" that can help high schoolers with their math studies and others to utilize math in everyday life applications.



At a suggested retail price of \$24.95, the kit is designed for students and others who want to make effective use of the calculator's capabilities in both classroom and home. It will be available through a wide variety of retailers.

For high school students, the new math kit will provide an opportunity for supplemental studies and exercises in algebra, trigonometry, physics, chemistry, probability and statistics. Ways to use the calculator to perform conversions are also included in the book since the metric system is now being adopted in the United States. Students are learning currently to measure gallons of gas in liters and distances in meters instead of feet or miles.

Students and others can also use the book and calculator on home management problems. For example, there are sample problems which show how easy it is to determine the amount of paint needed for a room area, quantity of fencing for yards or cement for patios. There are also hints for smart supermarket shopping including finding unit costs and managing a budget at the market.

Numerous other exercises and hints cover how to use the calculator in personal business and finance applications. Included are such things as credit card purchases, figuring mortgage points, interest cost, depreciation and foreign currency conversions.

The closing part of the book introduces the users to some entertaining puzzles and games they can enjoy with the calculator. Some examples are calculating biorythms, doing crossword puzzles and just having fun with numbers.

For further information contact Texas Instruments, Incorporated, P.O. Box 5012, Dallas, TX 75222; (214) 238-2481.

CIRCLE INQUIRY NO. 109

Slim Profile

The UNIVUE keyboard and instrumentation enclosure is designed for low profile instrumentation and computer data entry applications. Special design features include a welded .062

inch steel body of two piece construction for strength and an outside removable, flush mounting aluminum panel.



Overall size is 24"x12"x3", with front panel size of 23"x8". The UNIVUE body is coated with light gray lacquer type primer/surfacer to allow virtually any type paint to be used in the application of final finish. The UNIVUE is shipped complete with aluminum panel, rubber

feet, and mounting hardware. Shipping weight is 17 lbs., with delivery from stock. 1-24 price is \$32.95.

For further information contact Advanced Data Sciences, P.O. Drawer 1147, Marion OH 43302; (614) 382-7917.

CIRCLE INQUIRY NO. 110

Five New Convection-Cooled Switching Power Supply Models

Powertec now offers five new models of the industry's highest power density, off-the-shelf, convection-cooled switching regulated power supply series. Packaging density is achieved as a result of the mechanical configuration, and through utilization of a 40kHz switching rate - also the industry's first.

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200T24N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T25N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T26N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T27N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T28N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T29N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T30N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T31N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T32N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T33N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T34N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T35N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T36N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T37N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T38N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
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200T40N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T41N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T42N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T43N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T44N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T45N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T46N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T47N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T48N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T49N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T50N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
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200T52N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T53N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
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200T55N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T56N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T57N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T58N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T59N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T60N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T61N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T62N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T63N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T64N	17	5N7A14LN	2.20	ME565V	1.25	40D07	85	8728	2.75
200T65N	17	5N7A14LN	2.20</						

[illegible]

		1	2
MM5262	2K RAM	1.90	
MM5369	Divider	2.10	1
2102-1	500 NS 1K RAM	1.80	1
MM5375AA	Alarm Clock	3.75	2
FND503	50" Display	1.20	
18MHz	Crystal	3.90	2
PD411-J	150 NS 4K RAM	8.00	5
MA1002E	5" Alarm Clock Mod	8.95	7
MA1013E	7" Alarm Clock Mod	10.95	8
MM5309	Clock	3.90	2
MM5314	Alarm Clock	3.90	2

* Other parts, also avail.

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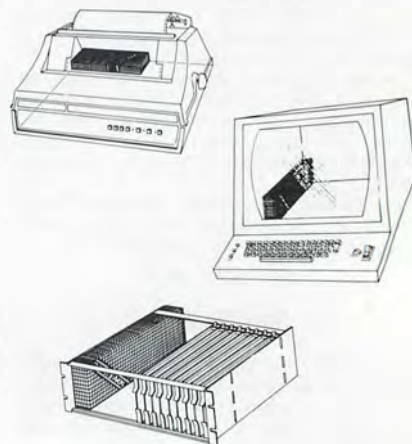
Includes everything except case. 2-PC boards. 6-.50" LED Displays. 5314 clock chip, transformer, all components and full instructions. Same clock kit with .80" displays **\$22.75**

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CDP1802 \$29.50 Users Manual 7.50
Complete kit of parts to build the "Elf" incl. CDP 1802 and users manual as listed in Aug. '76 Pop. Elect. minus power supply and board \$92.00



This supply in unit quantities sells for \$395, which makes it one of the least expensive



switching supplies available in this power range. Units have been provided to Underwriters' Laboratories for investigation and recognition per UL478 & UL114. Units are available for demonstration and evaluation now with production quantities available in October.

For complete details and specifications on the 9E Series, send for the new "Contortionist" brochure.

For further information contact Powertec, Inc., 9168 De Soto Avenue, Chatsworth, CA 91311; (213) 882-0004.

CIRCLE INQUIRY NO. 111

Prompting Desktop Programmable Calculator

A prompting programmable desktop calculator featuring a display that communicates with the user has been introduced by Texas Instruments Incorporated. The desktop SR-60 includes a printer, magnetic card reader and more individual function keys than any other calculator.



With its "prompting" display, an SR-60 user can run alphanumeric programs which request information through the 20-character display at successive stages in a problem. The calculator then waits for a response before continuing with problem solving. This "dialogue" allows even a novice to work with complicated problems immediately.

The SR-60 is designed for both business and technical operations. In business, it is capable of many functions, including financial analysis, long-term forecasting, and payroll. In technology, its 46 exposed scientific functions are immediately available for calculations, and 480 program steps, expandable to 1920 with an optional module, are available for complex programming.

Although it has high programming capability, the SR-60 can also be operated easily as a general purpose calculator. Its left-to-right algebraic entry and 9 levels of parentheses allow problems to be entered exactly as a user would say them. Answers can then be displayed, printed, or both — at the user's option.

The wide range of keyboard functions includes trig functions, hyperbolics, powers, roots, logs, $\Delta\%$, factorials and many other mathematical functions. Degrees of accuracy can be precisely controlled to provide intermediate rounding, decimal variance, and scientific notation.

Extra functions such as conversions, random number generation, and standard deviations are available in pre-programmed applications packages. The full alphabet is included in the keyboard, which is used for making display-prompting programs and for convenient labeling of printout sections.

The basic calculator has 480 program steps and 40 data memories, and retails for \$1695. The expanded memory option retails at \$300.

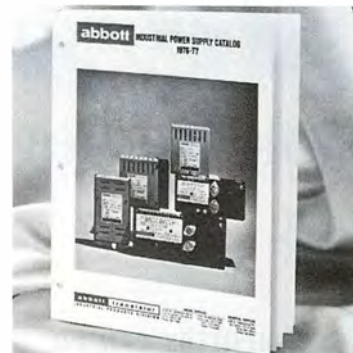
For further information contact Texas Instruments, Inc., Post Office Box 5012, Dallas, TX 75222 (Attn: SR-60).

CIRCLE INQUIRY NO. 112

LITERATURE

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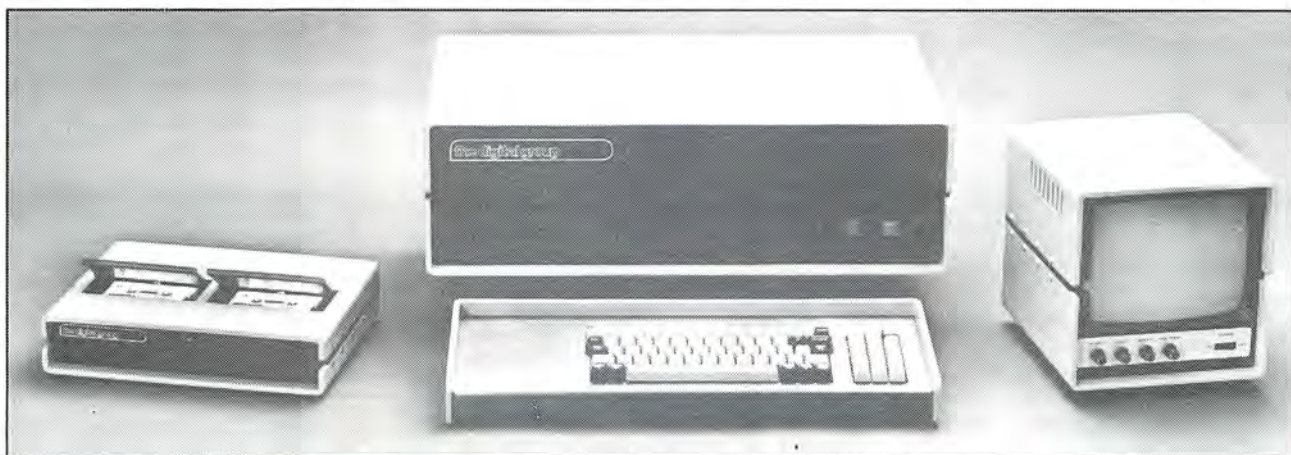


This informative catalog has been expanded and contains complete physical and electrical specifications on our lines of AC to DC power supplies and DC to AC power inverters for industrial and OEM applications. All units are high reliability, rugged modules with built-in quality. Prices are listed with each model with discounts to 99 pieces shown.

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CIRCLE INQUIRY NO. 113

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Book Review

WHAT COMPUTERS CAN DO

By Donald D. Spencer

Camelot Publishing Co., Inc., 1977

Paperback

*Review by
Judy Scolney Robertson &
Larry Robertson*

What Computers Can Do is a general overview of the "practical applications of the computer and how it aids people in their everyday work." The book is aimed at a juvenile audience. It presupposes no familiarity with computers on any level and concentrates on a discussion of the various areas in which computers are used, saying very little about programming, design nor electronics.

Aside from the use of an occasional buzz word (e.g. "analog to digital," "transducer"), Spencer's approach is totally non-technical. Spencer covers numerous computer applications in this illustrated paperback. He includes education, banking, medicine, art, engineering, music, law enforcement, government, recreation and the media, as well as several other areas. In addition, Chapter 2, "The Computer Threat to Society," addresses such current problems as privacy and privileged information, the misuse of computers and the effects of automation on employment. This chapter is of particular interest to the young reader who will soon be emerging into a computer-dominated society.

Computers is a well-written introductory book for the preteen or teenager with no previous exposure to our friendly machines. However, the book could be improved by the in-

clusion of a definition of each technical term, either as it occurs or in an appended glossary. The illustrations, mostly photos, are interesting, but with the green on green printing, they are often poorly reproduced. Replacement of some photos with line drawings or cartoons would have significantly enhanced the book. This does not prevent us, however, from recommending *What Computers Can Do* as a fine answer to the question, "Why do we have to have computers?"

VOLTAGE REGULATOR HANDBOOK THEORY AND PRACTICE

Henry Wurzburg,
with contributing authors
Bernie Montoya, Cal Lidback
and Nick Lycoudes

Motorola Inc., 1976

Price: \$2.50

Paperback. Available through Motorola distributors or by writing directly to Motorola Semiconductor Products Inc.

*Review by
Judy Scolney Robertson &
Larry Robertson*

The *Voltage Regulator Handbook* is a comprehensive guide to the use and functions of voltage regulators. Aimed at the electrical engineer, it is still comprehensible to the sophisticated hobbyist with a thorough knowledge of electronics. Written and published by Motorola Semiconductor Products Inc., the *Handbook* relies heavily on Motorola products in its detailed explanation of the operation of the voltage regulator. Motorola data sheets which are complete, clear and well designed are included in this highly technical manual, as is an industry-wide cross reference guide.

The need for voltage regulators is best stated in the preface, as well as a brief history and commentary on recent developments in the field:

In many electronic systems, voltage regulation is required for certain functions. Yesterday's voltage regulators were often complex and expensive circuits. Valuable time was diverted from the major system development effort to design the voltage regulators. Today's monolithic integrated circuit (IC) regulator is easing that task. Available as a growing variety of special-function devices and with fixed

and adjustable voltage ranges, the IC regulators offer design simplification and dramatic cost improvements.

Wurzburg, et al., more than adequately cover basic theory, selection of regulators, circuit configuration, design considerations, heat sinking, reliability, design and layout. In addition, special sections are devoted to trouble shooting and design of the input supply.

The *Handbook* is a totally professional publication, easy to refer to and to use. Additional sources are listed where appropriate, allowing the interested reader to find further data on the subject easily.

The *Voltage Regulator Handbook* is an exceptional reference for the use of voltage regulators. It would be a valuable, if not vital, addition to the technical library of anyone engaged in the selection and use of IC voltage regulators.

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CIRCLE INQUIRY NO. 41

THE BLACK

Imagine a black box. On one side is a switch, on the other a light. The switch has two positions, up and down. Place the switch up and the light comes on. Place it down and the light goes off.

Figure 1

Now try to imagine what is going on inside the box. First there might simply be two wires connecting the switch to the light. There is also the possibility that the switch does not connect directly with the light, but that it turns on a light inside to which a trained rat responds by running over and turning on another switch that turns on the outside light. A third possibility is that there is a human being inside the box who responds to an inside light in the same way the rat does.

These three possibilities demonstrate that there is more than one way of internally structuring a device to perform the same input-output function. A couple of important differences exist in these three forms.

One is speed. The wired switch turns on the light fastest in response to the switch being thrown. The rat is probably second in speed and the human is the slowest.

Figure 2

If the creator of the black box wanted to change the input-output function (e.g. to have the light go off when the switch is up and on when down), he would face different degrees of difficulty. In the wired case, he manually would have to change the connections between the switch and the light. In the rat example, he might either place a new rat in the box, trained in the opposite way, or quickly retrain the present one. For the human, he might simply say to him, "Okay, do it the other way," (being sure to specify exactly what is meant by "the other way").

These differences are for time and ease of change only; the input-output function remains the same. If one has ever used a computer system via a remote terminal or by passing cards and printout back and forth through a window, he cannot tell for sure whether the program went through a computer, whether a human figured out the answer and typed it back, or whether a highly trained rat responded to the input with a pre-learned response. In analogy, software and hardware and their in-between mixture, firmware, perform the same logical function. Their only difference is in speed and ease of change.

There is a second type of black box. This is one whose output is dependent not only upon the present input, but upon inputs which occurred in the past. For example, assuming the black box has the property that for every third time the switch is placed in the up position, the light is turned on, and it turned off the next time the switch came down. The sequence of events inside the box might be: "The switch is up, that's one. Now it's down. Now it's up, that's two. Now it's down. Now it's up again, turn on the light. Now it's down, turn the light off and start over."

Figure 3

This sequence may be viewed as a series of transformations in which the box's input-output function changes. Initially it is a box waiting for three "switch-ups" to occur in order to turn on the light. Once the switch has been thrown up, it is a box waiting for two more "switch-up's" before turning on the light. The second time the switch is thrown up, it is a box needing one more "switch-up." The third time the switch is put up, it is a box with the light on and requiring a single "switch-down" to turn it off.

Each of these forms represents the concept of a state. For each state, the response to present and

SW	Light
Up	On
Down	Off

Figure 1.

SW	Light
Up	Off
Down	On

Figure 2.

BOX

By KENNETH PUGH

future input differs. A state is dependent upon both the internal arrangements of the box and all previous inputs. A change in state may be considered as either a reconfiguration of the internal workings of the box or as some sort of memory (e.g. an "up-switch" counter).

There is a third type of black box which differs slightly from the previous ones. Suppose there was an additional input to the box which signaled to the internal operator that it must look at the input only when this additional input went from down to up or up to down. At any other time, the original input could be switched up and down and the state of the box and the light output would not be affected. This additional input signals the passage of time in the sense it tells the box the time at which to look at the other input. Thus it is commonly called a clock. Boxes whose state changes only when the clock is toggled (when signal goes from up to down or down to up) are termed synchronous. Most logic is built synchronously to avoid problems that occur when physical functions and interconnections are implemented.

Figure 4

One can explore the computer using the black box analogy in many ways, for it is nothing more than a complex interconnection of black boxes. Inputs may be represented by switches on a front panel, or a keyboard, or by electrical voltages or currents. Outputs may be lights or printed characters or electrical voltages or currents.

The designer of integrated circuits look at various silicon configurations as black boxes, providing input-output functions on a microscopic level. The logic designer uses the integrated circuits as black boxes to be interconnected to form a computer. The computer user may view the entire computer as a black box with a complex function of output versus input.

SW	# of 'UP'S'	Light
Down	0	Off
Up	1	Off
Down	1	Off
Up	2	Off
Down	2	Off
Up	3	On
Down	3	Off
Up	1	Off
	and so on	

Figure 3.

A computer user prepares a BASIC program to add two input numbers together and to print out the sum. He starts the computer and branches to a loader routine. By inputting the command "Load," he configures the computer into a black box that simply reads a binary input (the BASIC interpreter) and remembers it. By typing the input "Go," he changes the computer into a box that interprets his typed inputs as BASIC statements and remembers them. By typing "Run," he then changes his computer into a box that takes the next two inputs, adds them, and prints out the result.

The computer hobbyist may apply the black box approach on several levels; he can use a micro-processor circuit as a black box with its given input-output function and set of states defined by its internal registers, or he may buy a pre-built computer system and use it as a black box. He can buy a stored program in PROM (programmable read-only memory) and use it as a box to perform its function. Or he may use pre-written software (as a BASIC interpreter) as a black box.

One need not have any knowledge of an entire computer and a BASIC interpreter to use the BASIC language. By treating entire system as a set of black boxes, one can select those whose internal functions one wishes to understand and those which will be put to use.

The modern computer makes no distinction between instructions, which configure the device into a different black box, and data, which is input to the black box. Thus there is an ambiguity as to whether the computer responds to an input by changing itself into a different box or whether it simply remembers the past input. In either case, it can be considered a change in state.

Editor's note: ... and from this series of micro-cosmic events, our lives in the everyday mesocosm have been irrevocably altered.

SW	Clock	Interval State
Up	↓	Previous
Up	↑	Up
Down	↓	Previous
Down	↑	Down

based on positive edge
triggered service

Figure 4.

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CIRCLE INQUIRY NO. 49

Software Section

ALL MICROCOMPUTER MAGAZINES ARE NOT EQUAL

Contrary to Wayne Green's (Publisher of Kilobaud Magazine) generalized prognosis about microcomputer magazines not publishing long software programs nor paying more than \$50.00 for software programs, other microcomputer magazines have been doing this for some time now. KILOBAUD's apparent policy of not publishing long programs nor paying more than \$50.00 for a software program article in no way establishes the trend at the publishing market place.

BYTE, Dr. DOBB'S JOURNAL & INTERFACE AGE all have published long software programs in the past. Although I cannot speak for the other microcomputer magazines, INTERFACE AGE will continue to publish long programs. A good example of this is the 1976 December issue of INTERFACE AGE. This issue included the following software articles:

- Mark Borgerson's, Test Editor for the SWTPC-6800 software article consisting of 6½ typeset pages including a 605 line statement source listing program;
- Roger Rauskolb's Dr. Wang's Palo Tiny BASIC software article consisting of 10 typeset pages including grammar and over 1700 line statement source listing program;
- Four part serial LLL BASIC Interpreter software article that includes grammar and complete source listing program with over 200,000 bytes of source code that probably will require well over 50 typeset pages to publish.

Both of the other microcomputer magazines also have published meaningful long programs.

In regards to total payment for long software programs both BYTE and INTERFACE AGE are paying up to \$50.00/typeset page for software manuscripts (Dr. Dobb's Journal current policy is not to pay for manuscripts published). Even a six year old would tell you that \$50 times say 10 pages is more than \$50 which is apparently the maximum price that KILOBAUD would pay for this software article.

To draw your own conclusions as to which microcomputer magazine to submit your software programs please refer to the following columns in this issue of INTERFACE AGE:

- INTERFACE AGE'S Best Article of the Month Award.
- INTERFACE AGE Will Pay Up to \$50/Page for Software
- Best Article Of the Year Award

INTERFACE AGE IS FILLING THE SOFTWARE VOID WITH MAJOR PROGRAMS

INTERFACE AGE is filling that microcomputer software void. This issue includes six articles on software featuring a major stock investment program, and six software development programs. These programs are:

- The stock option program by Edward Christianson

provides microcomputerized *Hedge* Options for the sophisticated stock investor. This software article includes fundamentals and presents stock investment strategies required to be successful at the market place. The software program is written in Processor Teck's 5K BASIC for the 8080 microcomputer

- A Random Number Generator assembly language program by Bob Martin provides an improved RND Function Generator for your 8080 BASIC Interpreter. In addition a RND Function Generator *Chi-Square* test program is included to help you determine just how good is your RND Function Generator.
- An 8080 Memory Object Code Search Routine in assembly language by T. E. Travis provides means for searching unknown object code for known instruction sequences in order to modify object coded software to be compatible with your system or to add software embellishments.
- A resident 6800 development software monitor program called PROTO developed by and made available to the readers of INTERFACE AGE by American Microsystems. PROTO is a ROM resident monitor firmware package that comes with AMI's EVK series of microcomputer boards.
- A BASIC Floating Point Math Package by David Mead and others for the LLL BASIC Interpreter is presented in this issue. This is part #3 of the series of articles on the LLL BASIC Interpreter program.

CALL FOR INFORMATION ON BASIC PROGRAMMING LANGUAGES

INTERFACE AGE is conducting a survey on the characteristics and programming power of microcomputer BASIC conversational programming languages. This survey includes Tiny BASIC (TB), Tiny BASIC Extended (TBX), Standard BASIC (SB), Standard BASIC Extended (SBX) and Business BASIC (BB) languages. One of the many objectives of this survey is to highlight the correlation between BASIC languages in order to provide insight for running a BASIC application program on any of the different BASIC languages. At the completion of this survey, the results will be published in INTERFACE AGE.

If you have developed, helped develop, or modified any BASIC type of programming language for any microcomputer, please contact or send hard copy of grammar, user's manual, copy of software and any supporting documentation to Robert A. Stevens, software editor, INTERFACE AGE. Please include your home and work telephone numbers (for coordination) with all correspondence.

BEST ARTICLE OF THE MONTH AWARD UP-DATE

INTERFACE AGE will bestow an Honorary Award of \$100.00 to the author of the best non-commercial microcomputer article of the month. Only individuals are eligible for this monthly honorarium. This monthly

award is in addition to the honorarium given on the page count basis. Microcomputer articles may be on hardware, software or a combination hardware-software and will be judged by the INTERFACE AGE readership.

INTERFACE AGE NEEDS YOUR VOTE

Help INTERFACE AGE determine the type of articles you want to see published in the future by casting your vote of 10 points for the article (block voting) or articles (by vote splitting) you liked best. Feedback will provide encouragement to authors and will help make the INTERFACE AGE The Microcomputer magazine of the industry.

Each INTERFACE AGE magazine shall include one original bingo voting card. Each individual possessing a bingo voting card shall be allowed up to ten votes to be cast as a total single vote block for one author or subdivided into any vote block segment size combinations, with the total cast vote sum not to exceed ten, cast between two or more authors (no xerox copies of the bingo vote card please). Each published article is assigned a block of 10 bingo card numbers with the last digit of the number (LSD) to represent your cast vote value. 0 represents a vote value of 10. The prefix digits of the number block defines the article number.

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INTERFACE AGE will bestow an Honorary Award of \$500 value in products advertized in INTERFACE AGE to the author of the best non-commercial microcomputer article published during the year ending November 1977. The best article of the year award will be picked from the group of the best article of the month awards. Like the best article of the month award, only individuals are eligible for this yearly honorarium. The yearly award is in addition to the monthly award and honorarium given on the page count basis. The yearly award will be judged by the editors of INTERFACE AGE and will be announced in February 1978 issue of INTERFACE AGE.

INTERFACE AGE WILL PAY UP TO \$50/PAGE FOR SOFTWARE

INTERFACE AGE is continually soliciting original unpublished quality documented highly commented source/object code software listings and software technical articles for publishing in the INTERFACE AGE. Manuscript text must be typed double spaced with wide margins. Figures, tables, flow diagrams and charts must be numbered and submitted on separate sheets of white bond paper (Send original copy only). Program listings must be printed on white clean paper using a new black ink ribbon, and please, if possible, supply a punched paper tape assembly (source + object) code listing + source code listing + object code

dump with your hard copy. Be sure to record your name, company and office and home telephone numbers on all materials submitted to the software editor. Also include statement in cover letter allowing INTERFACE AGE and the Microcomputer Software Depository to publish and distribute copies of your software program. Include a prepaid postage stamped envelope with your return address only if you want your manuscript returned, in the event that the submitted article is not accepted for publication.

Articles accepted and published will receive an honorary recognition award. Honorariums are based upon technical content, manuscript preparation and subject suitability for publication in INTERFACE AGE. Honoraria range from \$15.00 to \$50.00 per typeset magazine page. In addition, the best article of the month submitted will receive a \$100 bonus. INTERFACE AGE'S readership will determine by vote which is the best article. (See best article of the month award). All software submitted to INTERFACE AGE will be deposited in the Microcomputer Software Depository (MDS) for low cost distribution.

Address all software correspondence to R. A. Stevens, Software Editor, c/o INTERFACE AGE Magazine, 2361 E. Foothill Blvd., Pasadena, CA 91107 or call (213) 449-1655.

SOFTWARE SHOPPING LIST

Now that INTERFACE AGE has expanded the microcomputer software coverage and developed a large appetite for good software, your programs and application software is badly needed to sate this enlarged software appetite. This software shopping list includes the following:

- **Microcomputer Development Software** such as assemblers, disassemblers, editors, monitors, utilities, mini-maxi BASIC interpreters and compilers, FORTRAN interpreters and compilers, boot strap loaders, software drivers, cassette software operating systems (COS), floppy disc software operating systems (FDOS), TTY software operating systems (TTYOS), and CRT software operating systems (CRTOS) for all microcomputer configurations.
- **Short Software Routines** such as math packages and I/O diagnostics for all microcomputer configurations.
- **Application Software Programs** such as Analog To Digital Converter (DAC) - Digital to Analog Converter (DAC) software control programs, Automated membership billing and mailing list update program, Inventory control software, invoice and billing software. Accounts Receivables and Payable software, process control programs, etc. for all microcomputer configurations.
- **Software Communications Protocol Programs** for such communication protocols as the BSC or Bisync (Binary Synchronous communications protocol procedures) and the new SDLC (Synchronous Data Link Control communication protocol procedures), etc.
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ing formats.

- **Microcomputer Game Programs**
- **Add Your Own Program Shopping List Here** Send your list to the software editor.

HALF SIZE PROGRAM LISTINGS VS FEWER PROGRAMS UPDATE

Starting with this issue full size xerox copies of software published in half size format will be available from the Microcomputer Software Depository (MSD). See MSD program listing for details.

INEXPENSIVE MICROCOMPUTER SOFTWARE

The Microcomputer Software Depository (MSD) will act as repository for source and object code tapes. Programmers wishing to contribute programs to the public domain but who do not want to bother with distribution, may do so by forwarding appropriate documentation including short descriptive write-up and punch paper tape copy of program if possible or cassette copy to MSD. There is no membership fee for access to the public domain paper tapes (PDT) from MSD.

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PROGRAM MEDIA

PTAC PAPER TAPE ASSEMBLY CODE
PTSC PAPER TAPE SOURCE CODE
PTOC PAPER TAPE OBJECT CODE

PTBC	PAPER TAPE BASIC CODE
PTAL	PAPER TAPE ASSEMBLY LISTING
PTSL	PAPER TAPE SOURCE LISTING
PTOL	PAPER TAPE OBJECT LISTING
PTOD	PAPER TAPE OBJECT DUMP
PTBL	PAPER TAPE BASIC LISTING
CTAL	CASSETTE TAPE ASSEMBLY LISTING
CTSL	CASSETTE TAPE SOURCE LISTING
CTOL	CASSETTE TAPE OBJECT LISTING
CTOD	CASSETTE TAPE OBJECT DUMP
CTBC	CASSETTE TAPE BASIC CODE
CTBL	CASSETTE TAPE BASIC LISTING
HCAC	XEROX HARD COPY OF ASSEMBLY CODE
HCSC	XEROX HARD COPY OF SOURCE CODE
HCOC	XEROX HARD COPY OF OBJECT CODE
HCBC	XEROX HARD COPY OF BASIC CODE
HCAL	XEROX HARD COPY OF ASSEMBLY LISTING
HCALF	FULL SIZE XEROX HARD COPY OF ASSEMBLY LISTING
HCSL	XEROX HARD COPY OF SOURCE LISTING
HCOL	XEROX HARD COPY OF OBJECT LISTING
HCOD	XEROX HARD COPY OF OBJECT DUMP
HCBL	XEROX HARD COPY OF BASIC LISTING
TEXT	XEROX HARD COPY OF PRINTED TEXT
PTTL	PAPER TAPE TEXT LISTING
CTTL	CASSETTE TAPE TEXT LISTING
MAN	MANUAL
HCGR	XEROX HARD COPY OF GRAMMAR
PTGR	PAPER TAPE COPY OF GRAMMAR
BBSL	XEROX HARD COPY OF BINARY BOOTSTRAP LOADER
HBSL	XEROX HARD COPY OF HEX BOOTSTRAP LOADER
PACK	PACKAGE PRICE INCLUDES ALL ITEMS/PROGRAM # WITH SYMBOL <

SUFFIX C = HAND ASSEMBLED CODE
SUFFIX L = COMPUTER FORMATED LISTING
SUFFIX D = CODE DUMP IN OCTAL OR HEX
SUFFIX F = FULL SIZE COPY

NOTES

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DEFINITIONS:

ASSEMBLY LISTING: COMPUTER ASSEMBLED SOFTWARE PROGRAM LISTING THAT INCLUDES SYMBOLIC ASSEMBLY LANGUAGE SOURCE CODED INSTRUCTIONS WITH COMMENTS PLUS EQUIVALENT MACHINE LANGUAGE OBJECT CODED INSTRUCTIONS AND MEMORY ADDRESS ASSIGNMENTS FOR EACH INSTRUCTION (SOURCE + OBJECT).

ASSEMBLY CODE: SAME CONTENT AS ASSEMBLY LISTING BUT HAND ASSEMBLED.

SOURCE LISTING: SOFTWARE PROGRAM LISTING RESULTING FROM COMPUTER SOFTWARE CONTROLLED ASSEMBLY PROCESS THAT INCLUDES ASSEMBLY LANGUAGE SOURCE CODED INSTRUCTIONS WITH COMMENTS. SOMETIMES, LINE STATEMENT NUMBERS ARE INCLUDED FOR EACH INSTRUCTION.

BRANCH TO PAGE 101

INTERFACE AGE 93



Have you ever been suspicious of the numbers that your version of BASIC pumps out for use in your favorite computer game? Maybe the royal rats are consistently eating too much grain in the game of KINGDOM, or possibly you think your shields are absorbing energy at an unreasonable rate in STAR TREK. If this sounds familiar, I suggest you pay a visit to your favorite psychiatrist and get checked out for a persecution complex. The only way you could guess that your random number generator was a lemon is if it were written by Maxwell's Demon, the infamous violator of the Second Law of thermodynamics.

Need A Better Random Number Generator?

By Bob Martin



There is a right number, a wrong number and a random number. But when is the right number a wrong number for a random number?



Having said that, I am going to claim anyway that I did detect a bad one in this manner. My guess that it was a bad generator, turned out to be correct. A few weeks back I wrote a Yahtzee game in order that my wife could play with the computer. (This is a good practice. It helps to reassure her that the money we spent on it was well worth it.) While checking out the game for errors I noticed, more often than I could believe, that the game ended with the sixes box empty. How many games with zero in the sixes box would be believable?

The RND function in BASIC returns a decimal fraction that lies between zero and one. Now suppose you have ten boxes and four red marbles . . . No wait! I'm not going to do that. Everybody falls asleep when the boxes and marbles are brought out. Let's assume that everyone reading this likes programming. Therefore we have an array of ten elements numbered zero through nine. All ten elements start out with the value zero. We will now call upon the RND function to decide which of the ten elements to increment by one. This is very simple. Just let $X = \text{INT}(10 * \text{RND}(0))$. X will now be the number of the element that is to be incremented. Now do this for, say, 1000 calls of RND. If RND generated truly random numbers, would it be believable if each element had the value 100? A person who had not studied elementary statistics might be surprised to learn that this would be very unbelievable.

To describe just how unlikely it is that the above result was produced by a truly random generator, let me change the outcome slightly. I will change it to a result that is much more likely to have been produced by a real random number generator. Suppose the ten elements turned out to have the following values: four of them were 95, four were 105, one was 99 and one was 101. A truly random RND function would give a result, this close to the expected result, only once in 100 trials of the experiment. (Each experiment, remember, was 1000 calls of RND.) Yet this modified result is very much more probable than the case where all ten elements have the value 100.

RND FUNCTION CHI-SQUARE TEST

You might wonder how such things can be deter-

mined. It is made possible by using one of the oldest statistical tests there is. This test is called the *chi-square* test and was introduced by Karl Pearson in 1900. We don't care right now why it works. Let that be a question to motivate the reading of some mathematics. For the present we only want to know if our random number generator can pass the *chi-square* test.

To make this test we must calculate a number called the *chi-square statistic*. This calculation is very simple for a random number generator. First, pick the number of categories you wish to use. In the above example the number was ten. Next choose the number of independent observations to be made. We used 1000. Now, since there are 1000 numbers that can fall into 10 categories, we would expect there to be 100 in each of them. We will call this the *expected* value even though we know better than to expect it too often. Take the *expected* value and subtract it from the value observed in each category. The observed values in the example above are the values that the elements of the array had after 1000 calls of RND. Take the result of each of these subtractions and square it. Now divide each of them by the expected value. To get the *chi-square statistic*, add all these numbers together. In the example above, you will have to sum ten numbers, one for each category. The *chi-square statistic* for the modified example above is 2.02.

HOW TO READ THE TEST RESULTS

Now you want to know what this number tells you about your random number generator. That's easy. It has all been worked out for you in a table. If you do not like tables, fear not. The *chi-square* distribution table is simple. The only thing you need to know is that (for our problem) the number of degrees of freedom is one less than the number of categories. We had ten categories, therefore we had nine degrees of freedom. Find the row in the table labeled with the number 9. This is the only row of data that will pertain to your generator. (You would use a different row if you had chosen a number of categories other than ten.) Now find the place your *chi-square statistic* falls in this row of data. Each number in the row also has a number at the top of its column. This is the number that interests you. It will be either a percentage figure or a decimal fraction less than one.

To illustrate, suppose your *chi-square statistic* is 2.09. Look for the number 2.09 in the row labeled 9. At the top of the column that contains 2.09 you will find either .99 or 99%. What this number means is the following: If your random number generator was truly random, then 99% of the time it would produce a number greater than 2.09. It is now up to you to decide if this is sufficiently random for your intended use of the generator. Since 99% is most of the time, you probably would not accept this. The same goes for the other end of the row. If you came up with the figure 1%, it would mean the ideal generator would get a *chi-square* larger than yours only 1% of the time.

A simple way to proceed is to declare the generator is acceptable if it falls within the 95 to 5 percent range. For the 9 degrees of freedom we have been using, this amounts to saying we will accept the generator if it can produce a *chi-square statistic* that lies between 3.3

and 16.9. The BASIC program given below may be used to test your random number generator. It uses 10,000 trials of RND and puts them in 10 categories. Notice that the number of trials has no effect on how the table is used. Only the number of degrees of freedom is important.

I tried this program with my three versions of BASIC. The results were so poor (*chi-square* of 217 was typical) that I had to recheck the *chi-square* program for errors. A moment's thought, of course, will give the reason why they were all so poor. Why take up more space than you have to in a BASIC interpreter, if most people only use RND to play STAR TREK? I can think of a couple of possible reasons; one is that someday you might want to use RND for something besides playing games. Another is that a bad RND might cause you to lose more games than is good for your self-image. Even if you do always win easily, the games will not be fun for long when you know that the reason you win is a faulty RND.

JUST HOW GOOD IS YOUR RND FUNCTION GENERATOR?

The bottom line is that it is simply more satisfying to have a good RND. Yahtzee feels better if you know your computer dice are as good as real ones. So try the test program (unless you wish to remain forever in doubt) and if your RND fails, I have a solution below for you. I might give one word of caution here that will serve as an incentive to read on. Even if your RND passes the test, it is not insured that your generator is perfect. There is a whole battery of tests that may be run. One such test is called the serial test which checks to make sure you don't have too many ascending or descending sequences of numbers. A so-called *feedback* generator will often fail this test. The generator I give below in 8080 code can pass many of the tests for randomness.

A BETTER RND FUNCTION GENERATOR

The method used here, to generate a sequence of random numbers, is a very common one called the mixed linear congruential method. It works like this. The previous random number (you must supply the very first number called the *seed*) is multiplied by a number called the *multiplier*. To this is added another number called the *constant*. Then still another number called the *modulus* is repeatedly subtracted from the result until the result is less than the *modulus*. This will then be the new random number. The whole process is repeated over and over, producing a sequence of numbers all of which are less than the *modulus*. If each new random number is always divided by the *modulus*, the result will be a sequence of numbers that are just what RND is supposed to produce, a sequence of random numbers that all lie between zero and one. It will be a random sequence provided that *multiplier*, *constant* and *modulus* are chosen properly.

A look at the 8080 RND function generator program will reveal two familiar strings of digits used for the *multiplier* and *constant*. The number used for the *modulus* is 2 raised to the 35th power. This makes it especially easy to do the repeated subtraction of the *modulus* when the arithmetic is done in binary. In fact, it

There are many areas to consider for the implementation of a good random number generator

doesn't need to be done at all. Just ignore all bits higher than 35 and the *modulus* operation is taken care of automatically. Since the number of bits is finite we cannot produce an infinite sequence of numbers. At some point the generator must repeat a number that was produced earlier. When this happens the whole pattern will also be repeated because the current number is always constructed from the immediately preceding number.

The above generator will give through all possible 35 bit numbers before it repeats. You may have noticed that the *familiar* numbers used are not what they should be in the last digit of each. They were changed so as to meet the conditions of a theorem that guarantees the generator will go without repeating as long as possible. In this case it will run for about 2 to the 35th or 34 billion numbers. To call the RND function this many times on my little micro would consume 11 years of around-the-clock computer time. Of course a long period is no guarantee of randomness. Counting from zero to 34 billion gives a sequence of long period which is obviously not random. The parameters given above provide for both a long period and randomness.

APPLICATION OF RND FUNCTION GENERATOR

There are a couple of things you must know to use this generator. If you want to repeat a given sequence of numbers, then locations 29AB through 29AF must be initialized with the same number each time you want to run the sequence. The fact that a sequence is reproducible is the reason these generators are called *psuedo-random*. If you don't care about being able to repeat a sequence then don't worry about what *seed* is at these locations. Since the generator is of maximum period there is no *seed* than can get you hung up in a shorter period sequence.

Another thing to know concerns returning the random number to your BASIC interpreter. The last part of the routine converts the binary random number in 29AB - 29AF into a BCD number and puts it in locations 29B0 through 29B5. This number must now be made compatible with the floating point representation of your BASIC interpreter. This is necessary because the BCD number must be divided by the *modulus* so that the final result lies between 0 and 1. A better method is to multiply by the inverse of the *modulus* (2 to the minus 35th or 2.91038E-11). Jump to your routine that does this preparation and multiplication from location 299F. A return after the multiplication should return to whatever called RND.

Remember that if your BASIC uses only six significant digits then only six digits of the BCD number are required. This will mean that a given number returned by RND will show up more often than once every 34 billion calls. However the pattern in the sequence before and after it will be different.

RND FUNCTION APPLICATIONS

Now that you have a fairly decent RND, what can you do with it besides play games? One demonstration is a simple example of what is called a Monte Carlo simulation. Try to calculate the number Pi by using RND: Draw a unit circle. Enclose the circle with a

```

RND: CALL ZERO
      LXI H, MULT+3
      LXI D, RSPC+4
      MVI B, 5
      MVI C, 8
      PUSH B
      PUSH D
      PUSH H
      MOV A, M
      RRC
      MOV M, A
      JNC NOBT
      LXI H, -RSPC-1
      DAD D
      MOV B, L
      LXI H, 5
      DAD D
      LDAX D
      ADC M
      MOV M, A
      DCX H
      DCR B
      JNZ ADCL
      XRA A
      LXI D, RSPC+4
      MVI B, 5
      LDAX D
      RAL
      STAX D
      DCX D
      DCR B
      JNZ SHFR
      POP H
      POP D
      POP C
      DCR C
      JNZ SWD
      POP B
      POP H
      DCX H
      DCX D
      DCR B
      JNZ BITC
      ; ADD THE CONSTANT TO THE
      LXI B, CONS+3
      LXI H, WKSP+4
      XRA A
      MVI A, 5
      STA CNT
      LDAX B
      ADC M
      STAX D
      DCX B
      DCX D
      DCX H
      LDA CNT
      DCR A
      JNZ ACN
      ; CONVERT BIN
      CAL
      LXI
      LI
      P
2900 CDBB29
2903 21A529
2906 11AF29
2909 0605
290B 0E08
290D C5
290E D5
290F E5
2910 7E
2911 0F
2912 D22929
2913 2156D6
2916 19
2919 45
291A 210500
291B 19
291E 1A
291F 8E
2920 77
2921 2B
2922 1B
2923 05
2924 C21F29
2925 AF
2928 11AF29
2929 0605
292C 1A
292E 17
292F 12
2930 1B
2931 05
2932 C22E29
2933 E1
2936 D1
2937 0D
2938 C20E29
2939 C1
293C 2B
293D 1B
293E 05
293F 05
2940 C20B29
2943 01AA29
2946 21B429
2949 11AF29
294C AF
294D 3E05
294F 32BA29
2952 0A
2953 8E
2954 12
2955 0B
2956 1B
2957 2B
2958 3ABA29
295B 3D
295C C24F29
295F CDBB29
2962 11AB29
2965 1A
2966 0F
2967 0F
      ; CLEAR WORK SPACE
      ; POINT TO MULTIPLIER
      ; POINT TO LAST RND NUM
      ; SET BYTE COUNT
      ; SET BIT COUNT
      ; SAVE BYTE COUNT
      ; SAVE REG OF ADD
      ; CURRENT BYTE OF MULTIPL
      ; GET BYTE OF MULTIPLIER
      ; ROTATE IT
      ; PUT IT BACK
      ; JUMP IF NOTHING TO A
      ; LIMIT OF RND NUM
      ; CALC. COUNT TIL END
      ; SAVE COUNT
      ; RESULT GOES -
      ; 5 BYTES DOWN
      ; GET NEXT BYTE TO
      ; ADD TO RESULT
      ; SAVE IT
      ; NEXT BYTE OF RE
      ; NEXT BYTE TO A
      ; NEXT BYTE DOWN
      ; ONE BYTE NOT I
      ; LOOP IF NOT I
      ; CLEAR CARRY
      ; POINT TO ST
      ; SET COUNT
      ; GET NEXT B
      ; SHIFT LEFT
      ; PUT IT BA
      ; ON TO NE
      ; DCR COUN
      ; LOOP IF
      ; RESET
      ; RESET
      ; ONE P
      ; LOOP
      ; GET
      ; ANC
      ; DC
      ; I

```


SOFTWARE SECTION

square that touches it at four points. Now use RND, in a BASIC program, to shoot darts over the entire area of the square. Count both the total number of darts thrown and the number of these that fall inside the circle. The ratio of the darts inside to the total number is the same as the ratio of the area of the circle to that of the square. The area of the circle is just π and the area of the square is four. Therefore multiply the dart ratio by four to get π .

If you should want to try this, here are two things to make it easier. First, use only the first quadrant. Second, when deciding if the dart is inside or outside the circle, there is no need to take the square root (unit circle). When I tried this on my computer with 16,000 darts 14 different times, I got the following results: Old bad RND, $\pi = 3.07778$; New good RND, $\pi = 3.14128$. Both had a standard deviation of .01. This method may be used to find volumes, masses, centers of mass etc., on more complicated objects that cannot be calculated exactly by other means.

Here is one more application which, even though unrealistic, might give you some other ideas. Suppose you know the average lifetime and the standard deviation of the chips in your 65K memory system. As the time approaches for the end of the first lifetime, more and more chips must be replaced one at a time. You might wonder if there is a time when it would be cheaper to just replace all the memory at once. Factors that would influence you to make a total replacement are: (1) discount price on large quantity of chips; (2) no time is wasted hunting for bad chips. Of course this is unrealistic because these factors would have to be greatly exaggerated before even one total replacement would be considered reasonable.

One way you might want to simulate this problem is to consider each chip separately. As you come to each chip you want an answer to the question, "How long before this chip will break down?" To get the answer just use the BASIC subroutine given below. Pass it the mean lifetime of a chip (M1) and the standard deviation of this lifetime (D1) and it will return the amount of time until the next breakdown (X) for that chip. The subroutine uses the Center Limit approach to simulate a normal distribution with the given parameters. Now run through the history of each chip for a given period of time, say, five years. Record the cost of each individual breakdown and the cost of each replacement of all 65K. The number of times the 65K is replaced in five years is determined by the time between replacements that you have selected. Run through all the chips for the five year simulation with your first selection for this amount of time. Then try it again for another time; and another. Vary this time (in a systematic fashion) until the total cost of maintenance for a five year period is a minimum. When the minimum is found you have the answer to your problem.

SUPER RND FUNCTION GENERATOR

One final note. If by chance the given generator should fail to be random in some application you might dream up, there is a plan for the Super Random

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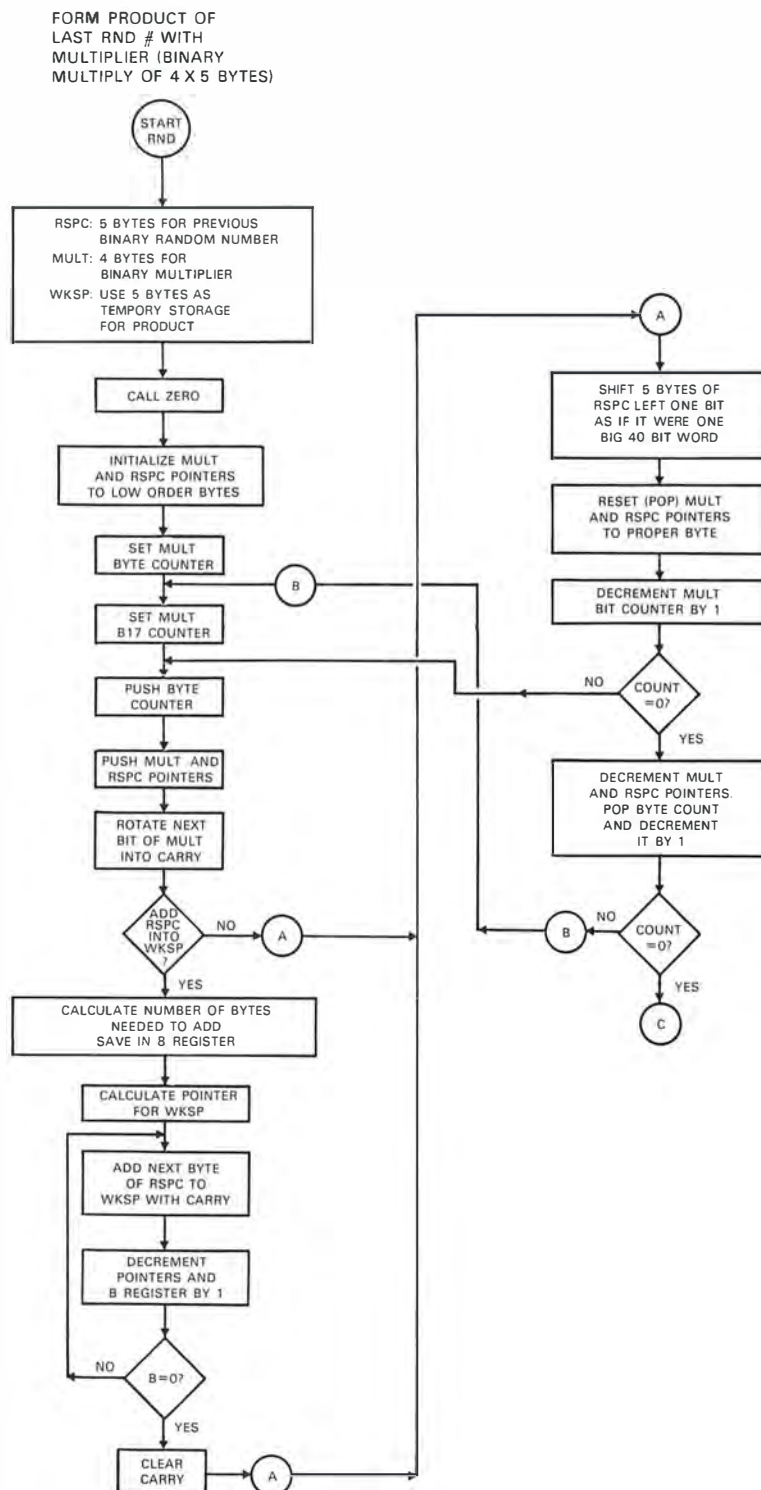
Number Generator. It was suggested by McLaren and Marsaglia and is said to meet anyone's criteria for *pseudo-randomness*. To accomplish this, two generators are required. Let the generator given above be called generator A. To construct generator B, simply exchange the values of *multiplier* and *constant* of generator A. Use generator A to lay out a list of about 100 random numbers. Use generator B to decide which of these 100 will be the next in our Super Sequence. The number which is used will be removed

from the list and replaced by a new number given by generator A. The whole process is repeated for the next number in the Super Sequence.

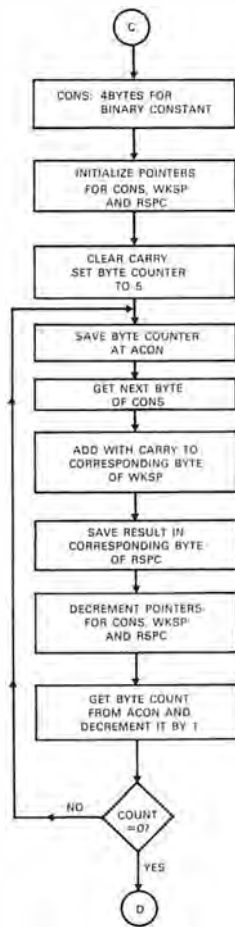
In summary I wish to encourage you to dump that old mantra you have been using and begin chanting RND to experience the true chaos of the universe.

**SEE MICROCOMPUTER SOFTWARE DEPOSITORY
PROGRAM INDEX FOR COPIES OF THIS PROGRAM**

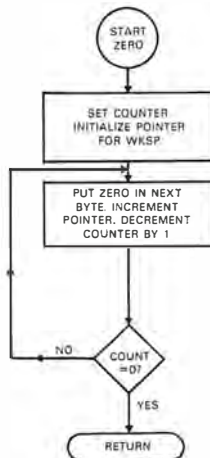
RND FUNCTION GENERATOR FLOW DIAGRAMS



ADD THE CONSTANT TO
THE RESULT (WKSP)
BINARY ADD OF 4 BYTES



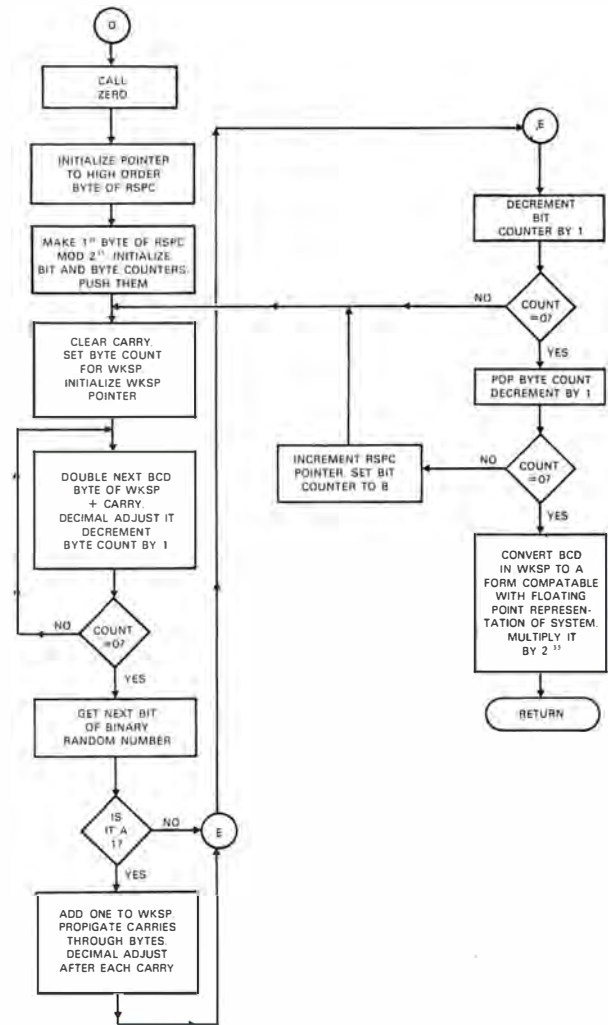
FILL WKSP
WITH ZEROES



Add the constant to the result (WKSP) binary ADD of 4 bytes

FEBRUARY 1977

CONVERT BINARY RANDOM
NUMBER TO BCD BY
POLYNOMIAL EVALUATION
USING HORNER'S METHOD



Convert binary random number to BCD by polynomial evaluation using Horner's method

INTERFACE AGE 99

RND FUNCTION GENERATOR PROGRAM

```

; TITLE /RANDOM NUMBER GENERATOR/
; THIS ROUTINE GENERATES RANDOM NUMBERS BY
; THE LINEAR CONGRUENTIAL METHOD (MIXED)
;
; FORM THE PRODUCT OF THE LAST RANDOM
; NUMBER WITH THE MULTIPLIER
;
2900 CDBB29 RND: CALL ZERO ;CLEAR WORK SPACE
2903 21A529 LXI H,MULT+3 ;POINT TO MULTIPLIER
2906 11AF29 LXI D,RSPC+4 ;POINT TO LAST RND NUM
2909 0605 MVI B,5 ;SET BYTE COUNT
290B 0E08 BITC: MVI C,8 ;SET BIT COUNT
290D 05 PUSH B ;SAVE BYTE COUNT
290E 05 SWD: PUSH D ;SAVE BEG OF ADD
290F 05 PUSH H ;CURRENT BYTE OF MULTIPLIER
2910 7E MOV A,M ;GET BYTE OF MULTIPLIER
2911 0F RRC ;ROTATE IT
2912 77 MOV M,A ;PUT IT BACK
2913 022929 JNC NOBT ;JUMP IF NOTHING TO ADD
2916 2156D6 LXI H,-RSPC-1 ;LIMIT OF RND NUM
2919 19 DAD D ;CALC. COUNT TIL END
291A 45 MOV B,L ;SAVE COUNT
291B 210500 LXI H,5 ;RESULT GOES -
291E 19 DAD D ; 5 BYTES DOWN
291F 1A ADCL: LEAX D ;GET NEXT BYTE TO ADD
2920 8E ADC H ;ADD TO RESULT
2921 77 MOV M,A ;SAVE IT
2922 2B DCX H ;NEXT BYTE OF RESULT
2923 1B DCX D ;NEXT BYTE TO ADD
2924 05 DCR B ;ONE BYTE DOWN
2925 C21F29 JNZ ADCL ;LOOP IF NOT DONE
2928 AF XRA A ;CLEAR CARRY
2929 11AF29 NOBT: LXI D,RSPC+4 ;POINT TO START AGAIN
292C 0605 MVI B,5 ;SET COUNT
292E 1A SHFR: LDAX D ;GET NEXT BYTE OF LAST RND NUM
292F 17 RAL ;SHIFT LEFT
2930 12 STAX D ;PUT IT BACK
2931 1B DCX D ;ON TO NEXT BYTE
2932 05 DCR B ;DCR COUNT
2933 C22E29 JNZ SHFR ;LOOP IF MORE
2936 E1 POP I ;RESET H TO MULTIPLIER
2937 D1 POP D ;RESET D FOR ADD
2938 0D DCR C ;ONE BIT OF MULT DONE
2939 C20E29 JNZ SWD ;LOOP IF NOT DONE
293C C1 POP B ;GET BYTE COUNT
293D 2B DCX H ;ANOTHER BYTE DONE
293E 1B DCX D ;ADD POINT MOVES DOWN 1 BYTE
293F 03 DCR B ;DCR COUNT
2940 C20B29 JNZ BITC ;LOOP IF MORE BYTES OF MULT
;
; ADD THE CONSTANT TO THE RESULT
;
2943 01AA29 LXI B,CONS+3 ;POINT TO CONSTANT
2946 21B429 LXI H,WKSP+4 ;RESULT OF MULT
2949 11AF29 LXI D,RSPC+4 ;PLACE FOR NEW RND NUM
294C AF XRA A ;CLEAR CARRY
294D 3E05 MVI A,5 ;SET COUNT
294F 32BA29 ACON: STA CMT ;SAVE IT
2952 0A LDAX B ;GET NEXT BYTE
2953 8E ADC M ;ADD THE PRODUCT
2954 12 STAX D ;SAVE RESULT
2955 0B DCX B ;BUMP
2956 1B DCX D ;ALL
2957 2B DCX H ;POINTERS
;
2958 3ABA29 LDA CNT ;GET COUNT
295B 3D DCR A ;DECREMENT IT
295C C24F29 JNZ ACON ;LOOP IF ANY LEFT
;
; CONVERT BINARY RANDOM NUM TO BCD
;
295F CDBB29 CALL ZERO ;CLEAR WORK SPACE
2962 11AB29 LXI D,RSPC ;POINT TO BIN RND NUM
2965 1A LDAX D ;GET FIRST BYTE
2966 0F RRC ;MAKE IT -
2967 0F RRC ;MOD -
2968 0F RRC ;2**35 (POWER)
2969 12 STAX D ;PUT IT BACK
296A 010305 LXI B,503H ;PREPARE TO JUMP -
296D C5 PUSH B ;INTO THE MIDDLE
296E C37529 JMP DLB1 ;DO IT
2971 13 DLB: INX D ;NEXT BYTE OF BIN RND
2972 C5 PUSH B ;SAVE BYTE COUNT
2973 0E08 MVI C,8 ;BIT COUNT
2975 AF DLB1: XRA A ;CLEAR CARRY
2976 0606 MVI B,6 ;BYTE COUNT FOR WKSP
2978 21B529 LXI H,WKSP+5 ;LOW ORD OF BCD RND NUM
297B 7E TTIM: MOV A,M ;GET NEXT 2 DIGITS
297C 8F ADC A ;DOUBLE THEM
297D 27 DAA ;MAKE IT DECIMAL
297E 77 MOV M,A ;PUT IT BACK
297F 2B DCX H ;MOVE TO NEXT HIGHER ORDER
2980 05 DCR B ;DCR COUNTER
2981 C27B29 JNZ TTIM ;LOOP IF MORE
2984 1A LDAX D ;GET BYTE OF BIN RND NUM
2985 07 RLC ;CHECK FOR BIT
2986 12 STAX D ;PUT IT BACK
2987 D29629 JNC MBT ;JUMP IF NO BIT
298A 21B529 LXI H,WKSP+5 ;BCD RND NUM
298D 7E PLUS: MOV A,M ;GET BYTE OF RND NUM
298E CE00 ACI 0 ;PROPAGATE THE CARRY
2990 27 DAA ;DECIMALIZE
2991 77 MOV M,A ;PUT IT BACK
2992 2B DCX H ;ONE DOWN
2993 DA8D29 JC PLUS ;DONE IF NOTHING TO CARRY
2996 0D DCR C ;DONE WITH 1 BIT OF BIN NUM
2997 C27529 JNZ DBL1 ;LOOP IF MORE IN THIS BYTE
299A C1 POP B ;GET BACK BYTE COUNT
299B 05 DCR B ;DECREMENT IT
299C C27129 JNZ DLB ;LOOP IF ANY LEFT
299F C3XXXJMP ;GOTO DIV ROUT.- U SUPPLY
29A2 BB40 MULT: DW 403BH ;3141592653
29A4 E64D DW 4DE6H ;THE MULTIPLIER
29A6 00 DB 0 ;ZERO NEEDED HERE
29A7 A205 CONS: DW 5A2H ;2718281829
29A9 B065 DW 65B0H ;THE CONSTANT
29AB DS 1 ;STORAGE FOR BIN RND NUM
29B0 WKSP: DS1 ;STORAGE FOR BCD RND NUM
29BA CNT: DS1 ;XTRA COUNT
;
; ROUTINE TO CLEAR WKSP
;
29BB 01000A ZERO: LXI B,0A00H ;COUNTER AND ZERO
29BE 21B029 LXI H,WKSP ;PLACE TO BE CLEARED
29C1 71 ZER1: MOV M,C ;PUT ZERO IN NEXT BYTE
29C2 23 INX H ;NEXT BYTE
29C3 05 DCR B ;DOWN WITH COUNT
29C4 C2C129 JNZ ZER1 ;LOOP TIL D'NE
29C7 09 RET ;BACK TO WO 'K

```

RND FUNCTION GENERATOR CHI-SQUARE TEST PROGRAM

```

5 REM CHI-SQUARE TEST
10 DIM A(9)
20 K=10
30 N=10000
35 REM ZERO THE ELEMENTS
40 FOR J=0 TO K-1
50 A(J)=0:NEXT J
55 REM LET RND FILL THE ARRAY
60 FOR J=1 TO N
70 B=INT(K*RND(0))
80 A(B)=A(B)+1
90 NEXT J
95 REM CALC. CHI-SQUARE
100 D=0
110 FOR J=0 TO K-1
120 C=A(J)-N/K
130 D=D+C*C
140 NEXT J
150 PRINT "CHI-SQUARE STATISTIC = ",K*D/N
160 STOP

```

```

500 REM THIS ROUTINE RETURNS A
501 REM NORMALLY DISTRIBUTED RANDOM
502 REM VARIATE WITH PARAMETERS D1 AND M1
505 X=-6
510 FOR K=1 TO 12
520 X=X-RND(0)
530 NEXT K
540 X=X*D1*M1
550 RETURN

```


VECTORED FROM PAGE 93

SOURCE CODE: SAME CONTENT AS SOURCE LISTING BUT HAND ASSEMBLED.

OBJECT LISTING: SOFTWARE PROGRAM LISTING RESULTING FROM COMPUTER SOFTWARE CONTROLLED ASSEMBLY PROCESS THAT ONLY INCLUDES MACHINE READABLE OBJECT CODED INSTRUCTIONS AND MEMORY ADDRESS ASSIGNMENTS.

OBJECT CODE SAME CONTENT AS OBJECT LISTING BUT HAND ASSEMBLED.

HARD COPY: XEROX OR PRINTED COPY

CODE: HAND ASSEMBLED CODE (SOURCE, OBJECT, OR ASSEMBLY CODE).

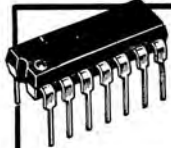
LISTING: COMPUTER FORMATED LISTING.

DUMP: COMPUTER MEMORY DUMP.

MSD PROGRAMS

CPU TYPE	SYMBOLIC NAME	DESCRIPTIVE NAME	MSD # & MEDIA	P R A E C V K	PRICE IN \$ *CALIF. TAX(+) *USA POSTAGE(++)			
6502	APPLECD	6502 APPLE COMPUTER DISASSEMBLER BY ALLEN BAUM & STEPHEN WOZNIAK-INTERFACE AGE, SEPT. 1976, VOL.1, #10.	1-TEXT 1-HCAL 1-PACK	< < +	2.00+0.12+1.00 INC. WITH TEXT			
8080	LPTIIF	LOAD 8080 PAPER TAPE IN INTEL HEX FORMAT BY BURT HASHIZUME-INTERFACE AGE, OCT. 1976, VOL.1, #11.	2-PTAL 2-TEXT 2-HCAL 2-PACK	< < < +	5.00+0.30+1.00 2.00+0.12+1.00 INC. WITH TEXT			
8080	HFVGA	8080 BINARY FILES WITH OPTIONAL AUTOSTART BY WILLIAM H. JORDAN-INTERFACE AGE, OCT. 1976, VOL.1, #11.	3-PTAL 3-PTOD 3-TEXT 3-HCAL 3-PACK	< < < < +	5.00+0.30+1.00 INC. WITH PTAL 2.00+0.12+1.00 INC. WITH TEXT			
8080	MINOPS	MIN OPERATING SYSTEM BY ED KEITH & DENNIS HESCOX-INTERFACE AGE, OCT. 1976, VOL.1, #11. PTAL+ INCLUDES OPERATING INSTRUCTIONS, PAPER TAPE FORMAT AND SAMPLE RUN	4-PTAL 4-PTOD 4-TEXT 4-HCAL 4-PACK	< < < < +	5.00+0.30+1.00 INC. WITH PTAL 2.00+0.12+1.00 INC. WITH TEXT			
8080	DBBDP	DR. BEATTIE'S BASIC DFT PLANNING BY DR. BEATTIE-INTERFACE AGE, OCT. 1976, VOL.1, #11.	5-TEXT 5-HCAL 5-PTBL 5-PACK	< < < +	2.00+0.12+1.00 INC. WITH TEXT 5.00+0.30+1.00			
6800	EZMERPS	ECHO 1, ZERO MEMORY, ECHO REVERSE & PRINT SUBROUTINES BY HOWARD BERENBON-INTERFACE AGE, OCT. 1976, VOL.1, #11.	6-PTAL 6-TEXT 6-HCAL 6-PACK	< < < +	3.00+0.18+1.00 1.00+0.06+1.00 INC. WITH TEXT			
8080	ESP-1	ESP-1 SOFTWARE PACKAGE BY MICHAEL SHRYVER-INTERFACE AGE, OCT. 1976, VOL.1, #11. PTGR IS PAPER TAPE COPY OF GRAMMAR.	7-PTOD 7-MAN 7-CTOD 7-MAN 7-PTGR 7-TEXT 7-HCAL 7-PACK	< + + + + + + +	30.00+1.80+1.50 INC. WITH PTOD 30.00+1.80+1.50 INC. WITH CTOD 5.00+0.30+1.50 INC. WITH PTGR INC. WITH MAN			
8080	PTSP-1	PROCESSOR TECHNOLOGY SOFTWARE PACKAGE NO. 1 SUMMARY BY R. A. STEVENS-INTERFACE AGE, OCT. 1976, VOL.1, #11.	8-PTTL 8-TEXT 8-PACK	< < +	4.00+0.24+1.50 INC. WITH PTTL			
8080	EXRAMMT	EXHAUSTIVE 8080 RAM MEMORY TEST PROGRAM BY T.E. TRAVIS-INTERFACE AGE, NOV. 1976, VOL.1, #12.	9-PTAL 9-PTOD 9-TEXT 9-HCAL 9-HCAL 9-PACK	< < < < < +	4.00+0.24+1.00 INC. WITH PTAL 1.00+0.06+1.00 INC. WITH TEXT INC. WITH TEXT			
6800	MEMDMP-1	SWTPC 6800 MEMORY DUMP PROGRAM MEMDMP-1 BY GARY KAY-INTERFACE AGE, NOV. 1976, VOL.1, #12.	10-PTAL 10-PTSL 10-PTOD 10-TEXT 10-HCAL 10-PACK	< < < < < +	3.00+0.18+1.00 3.00+0.18+1.00 INC. WITH PTSL 1.00+0.06+1.00 INC. WITH TEXT			
6800	ROBIT-1	SWTPC 6800 ROTATING BIT RAM MEMORY DIAGNOSTIC PROGRAM ROBIT-1 BY GARY KAY-INTERFACE AGE, NOV. 1976, VOL.1, #12.	11-PTAL 11-PTSL 11-PTOD 11-TEXT 11-HCAL 11-PACK	< < < < < +	3.00+0.18+1.00 3.00+0.18+1.00 INC. WITH PTSL 1.00+0.06+1.00 INC. WITH TEXT			
6800	MEMCON-1	SWTPC 6800 SHORT MEMORY ADDRESS CONVERGENCE PROGRAM MEMCON-1 BY GARY KAY-INTERFACE AGE, NOV. 1976, VOL.1, #12.	12-PTAL 12-PTSL 12-PTOD 12-TEXT 12-HCAL 12-PACK	< < < < < +	3.00+0.18+1.00 3.00+0.18+1.00 INC. WITH PTSL 1.00+0.06+1.00 INC. WITH TEXT			
6800	BJIB	BLACKJACK IN BASIC PROGRAM BY ED KEITH & DENNIS HESCOX. THE BJIB	13-PTBL 13-PTBL+	< +	5.00+0.30+1.00 6.00+0.36+1.00			
		PAPER TAPE OBJECT CODE REQUIRES ROBERT UITERWYK'S SWTPC MICROBASIC OPERATING SYSTEM-INTERFACE AGE, NOV. 1976, VOL.1, #12. PTBL+ INCLUDES SAMPLE RUN, INSTRUCTIONS, LIST OF VARIABLES AND LIST OF ROUTINES.	13-TEXT 13-HCBL 13-PACK	< < +	1.00+0.06+1.00 INC. WITH TEXT			
6502	RFRPR	REVISED FLOATING POINT ROUTINES FOR 6502* BY ROY RANKIN & STEVE WOZNIAK - INTERFACE AGE, NOV. 1976, VOL.1, #12. NOTE * - ORIGINAL MATH PACKAGE FIRST APPEARED IN DR. DOBB'S JOURNAL, AUG. 1976, VOL.1, #7. U.K. DOBB'S JOURNAL, AUG. 1976, VOL.1, #7.	14-PTOD 14-PTAL 14-PTSL 14-TEXT 14-HCAL 14-PACK	< < < < < +	3.00+0.18+1.00 9.00+0.54+1.50 9.00+0.54+1.50 2.00+0.12+1.00 INC. WITH TEXT			
6800	HISPDUMP	HIGH SPEED DOUBLE PRECISION MULTIPLICATION SUBROUTINE-HISPDUMP BY PERMISSION AND COURTESY OF MOTOROLA'S M6800 USER GROUP LIBRARY-INTERFACE AGE, NOV. 1976, VOL.1, #12.	15-PTAL 15-TEXT 15-HCAL 15-PACK	< < < +	4.00+0.24+1.00 1.00+0.06+1.00 INC. WITH TEXT			
6800	DIV16	REENTRANT 16 BIT DIVIDE SUBROUTINE - DIV16 BY PERMISSION AND COURTESY OF MOTOROLA'S M6800 USER GROUP LIBRARY-INTERFACE AGE, NOV. 1976, VOL.1, #12.	16-PTAL 16-TEXT 16-HCAL 16-PACK	< < < +	4.00+0.24+1.00 1.00+0.06+1.00 INC. WITH TEXT			
6800	RENTMUP	REENTRANT DOUBLE PRECISION MULTIPLICATION SUBROUTINE-RENTMUP BY PERMISSION AND COURTESY OF MOTOROLA'S M6800 USER GROUP LIBRARY-INTERFACE AGE, NOV. 1976, VOL.1, #12.	17-PTAL 17-TEXT 17-HCAL 17-PACK	< < < +	4.00+0.24+1.00 1.00+0.06+1.00 INC. WITH TEXT			
8080	HOMECD	COMPUTER OR CONTROLLER BY TERRY RENSON, INTEL - INTERFACE AGE, SEPT. 1976, VOL.1, #10.	18-PTAL 18-PTSL 18-TEXT 18-HCAL 18-PACK	< < < < +	3.00+0.18+1.00 3.00+0.18+1.00 1.00+0.06+1.00 INC. WITH TEXT			
8080	LCST	STARTREK BY LYNN COCHRAN-INTERFACE, JUNE 1976, VOL.1, #7.	19-PTBL 19-TEXT 19-HCBL 19-PACK	< < < +	5.00+0.30+1.00 1.00+0.06+1.00 INC. WITH TEXT			
8080	WSPG	WORD SEARCH PUZZLE GENERATOR BY RICHARD S. EDELMAN - INTERFACE, JULY 1976, VOL.1, #8.	20-PTBL 20-TEXT 20-HCBL 20-PACK	< < < +	4.00+0.24+1.00 1.00+0.06+1.00 INC. WITH TEXT			
8080	PGBIORHY	BIOKHYTHM BY PAUL GREEN - INTERFACE AGE, AUG. 1976, VOL.1, #9.	21-PTBL 21-TEXT 21-HCBL 21-PACK	< < < +	4.00+0.24+1.00 1.00+0.12+1.00 INC. WITH TEXT			
8080	WBIORHY	BIORHYTHMS IN PRACTICE BY WILLIAM L. DONHAN, M.D. - INTERFACE AGE, AUG. 1976, VOL.1, #9.	22-PTBL 22-TEXT 22-HCBL 22-PACK	< < < +	4.00+0.24+1.00 1.00+0.06+1.00 INC. WITH TEXT			
8080	REBJ	BLACKJACK BY RICHARD S. EDELMAN - INTERFACE AGE, AUG. 1976, VOL.1, #9.	23-PTBL 23-TEXT 23-HCBL 23-PACK	< < < +	5.00+0.30+1.00 1.00+0.06+1.00 INC. WITH TEXT			
8080	BLUFF	BLUFF BY PHIL FELDMAN & TOM RUGE - INTERFACE AGE, SEPT. 1976, VOL.1, #10.	24-PTBL 24-TEXT 24-HCBL 24-PACK	< < < +	5.00+0.30+1.00 1.00+0.06+1.00 INC. WITH TEXT			
6800	RABSMB	RELATIVE ADDRESS BACK-STEPPER IN MICRO-BASIC BY J. HUFFMAN - INTERFACE AGE, DEC. 1976, VOL.1, #13.	25-PTBL 25-HCBL 25-TEXT 25-PACK	< < < +	3.00+0.18+1.00 1.00+0.06+1.00 INC. WITH HCBL			
6800	TEFT6800	TEXT EDITOR FOR THE SWTPC-6800 BY MARK BORGESON - INTERFACE AGE, DEC. 1976, VOL.1, #13. HCAL IS COPY OF FULL SIZE ASSEMBLY LISTING.	26-PTAL 26-PTOD 26-HCAL 26-TEXT 26-PACK	< < < < +	10.00+0.36+2.00 5.00+0.30+1.25 26-HCAL 2.00+0.12+1.25			
8080	WPATBX	WANG'S PALO ALTO TINY BASIC BY ROGER RAUSKOLB - INTERFACE AGE, DEC. 1976, VOL.1, #13. HCAL & HCBL ARE COPIES OF FULL SIZE CODE	27-PTSL 27-PTOD 27-HCAL 27-TEXT 27-HCBL 27-PACK	< < < < < +	10.00+0.60+2.00 5.00+0.30+1.50 4.00+0.24+1.50 INC. WITH HCAL 4.00+0.24+1.50			
8080	LLLBI	LLL 8080 BASIC INTERPRETER GRAMMAR BY JERRY BARBER & ROYCE EDWARD - SUBMITTED BY E.R. FISHER - INTERFACE AGE, DEC. 1976, VOL.1, #13(PART 1). PART 2 PUBLISHED JAN. 1977, VOL.2, #1. TEXT1 IS PART 1, TEXT2 IS PART 2 AND HCAL2 IS FULL SIZE XEROX COPY OF BASIC ASSEMBLY LISTING WITHOUT FLOATING POINT.	28-TEXT1 28-HCAL2 28-TEXT2 28-HCAL3 28-TEXT3	< < < < <	2.00+0.12+1.25 5.00+0.30+2.00 2.00+0.12+1.25 5.00+0.30+2.00 2.00+0.12+1.25			
SC/MP	NIBL	NIBL-NATIONAL'S TINY BASIC GRAMMAR FOR SC/MP BY PHIL ROYAL - INTERFACE AGE, DEC. 1976, VOL.1, #13. ASSEMBLY LISTING PUBLISHED JAN. 1977, VOL.2, #1.	29-TEXT 29-HCAL 29-PTSL 29-PTOD 29-PTGR 29-PACK	< < < < < +	2.00+0.12+1.25 10.00+3.00+2.00 10.00+3.00+2.00 5.00+1.50+1.00 2.00+0.12+1.00			
SC/MP	MWBAGELS	BAGELS BY DR. MARVIN VINZINREAD BY PERMISSION & COURTESY OF NATIONAL SEMICONDUCTOR - INTERFACE	30-PTBL	<	2.00+0.12+1.00			

BRANCH TO PAGE 120

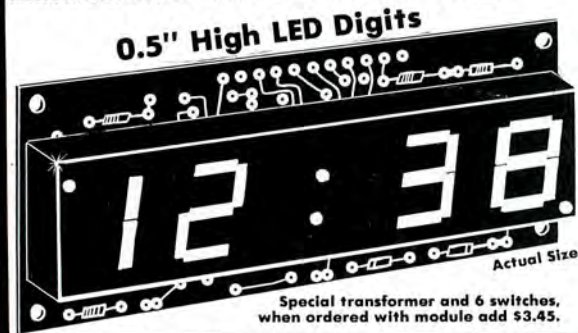


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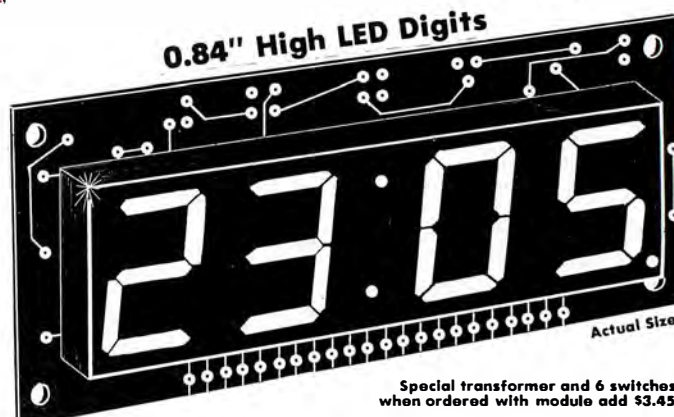
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The MA1002A and MA1010A have a 12 hour display with an AM and PM indicator. The MA1002C and MA1010C have a 24 hour display.

Features include alarm "on" and "PM" indicators, "sleep" and "snooze" timers and variable brightness control capability. The modules are extremely compact, the MA1002 measuring 1.375" by 3.05", the MA1010 measuring 1.75" by 3.75". This small size is achieved by bonding the I.C. to the back of the circuit board.

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RADIAL ELECTROLYTICS

47/50V . . . 08	65/10	22/50V . . . 12	1.00/10	330/25V . . . 23	1.86/10
1/50V . . . 08	65/10	100/6.3V . . . 09	75/10	470/10R . . . 21	1.71/10
22/50V . . . 08	65/10	100/10V . . . 10	77/10	470/16V . . . 23	1.81/10
33/50V . . . 08	65/10	100/16V . . . 11	85/10	470/25V . . . 29	2.35/10
47/50V . . . 08	65/10	100/25V . . . 10	85/10	1000/10V . . . 24	1.96/10
47/50V . . . 08	65/10	100/50V . . . 21	1.71/10	1000/16V . . . 29	2.35/10
10/16V . . . 08	65/10	220/10V . . . 13	1.08/10	2200/25V . . . 42	3.33/10
10/25V . . . 08	65/10	220/16V . . . 15	1.16/10	2200/10V . . . 42	3.33/10
10/50V . . . 08	65/10	220/25V . . . 21	1.71/10	2200/16V . . . 54	4.30/10
22/16V . . . 08	67/10	220/50V . . . 29	2.35/10	2200/25V . . . 58	4.67/10
22/25V . . . 09	70/10	330/10V . . . 15	1.16/10	3300/16V . . . 89	7.14/10
		330/16V . . . 21	1.66/10		

AXIAL ELECTROLYTICS

47/10V . . . 11	90/10	33/25V . . . 14	1.15/10	330/16V . . . 29	2.35/10
1/30V . . . 11	90/10	330/50V . . . 19	1.52/10	330/25V . . . 32	2.54/10
3/35V . . . 12	95/10	47/16V . . . 14	1.15/10	470/16V . . . 32	2.55/10
33/50V . . . 12	1.00/10	47/25V . . . 17	1.30/10	470/25V . . . 33	2.60/10
47/25V . . . 11	90/10	47/50V . . . 21	1.71/10	1000/10V . . . 33	3.00/10
47/35V . . . 12	95/10	100/10V . . . 14	1.13/10	1000/16V . . . 39	3.15/10
47/50V . . . 12	1.00/10	100/16V . . . 14	1.13/10	1000/25V . . . 56	4.50/10
10/25V . . . 12	1.00/10	100/25V . . . 20	1.55/10	2200/10V . . . 30	3.96/10
10/50V . . . 14	1.15/10	100/50V . . . 29	2.30/10	2200/16V . . . 62	4.95/10
22/16V . . . 12	1.00/10	220/10V . . . 18	1.42/10	2200/25V . . . 79	6.36/10
22/25V . . . 13	1.05/10	220/16V . . . 20	1.55/10	3300/16V . . . 95	7.63/10
22/50V . . . 17	1.32/10	220/25V . . . 29	2.35/10	4700/16V . . . 109	8.70/10
33/16V . . . 12	1.00/10	220/50V . . . 40	3.23/10	10000/10V . . . 115	9.19/10
		330/10V . . . 14	1.16/10		

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4-40 Hex Nut . . . 3.75M		4-40 Hex Nut . . . 3.75M	
6-32 Hex Nut . . . 60¢	4.00M	6-32 Hex Nut . . . 60¢	4.15M
8-32 Hex Nut . . . 60¢	4.15M		
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7406 . 25	7489 . 2.19	74190 . 1.23	4018 . 1.05	CA3046 .
7407 . 25	7490 . 44	74191 . 1.23	4019 . 23	LM2111N .
7408 . 21	7491 . 70	74192 . 88	4020 . 1.14	LM309K .
7409 . 21	7492 . 44	74193 . 88	4021 . 1.14	LM324A .
7410 . 21	7493 . 44	74194 . 88	4022 . 96	LM340T-5 .
7411 . 21	7494 . 70	74195 . 88	4023 . 23	LM340T-6 .
7412 . 21	7495 . 70	74196 . 88	4024 . 84	LM340T-8 .
7413 . 25	7496 . 70	74197 . 88	4025 . 1.14	LM340T-12 .
7414 . 89	74100 . 1.28	74198 . 1.49	4026 . 1.68	LM340T-15 .
7416 . 25	74107 . 30	74199 . 1.49	4027 . 40	LM340T-18 .
7417 . 25	74109 . 33	74201 . 1.09	4028 . 89	LM340T-24 .
7420 . 21	74121 . 35	74279 . 55	4029 . 1.14	LM3900N .
7421 . 25	74122 . 44	74365 . 67	4030 . 23	LM3909N .
7423 . 35	74123 . 61	74366 . 67	4033 . 1.51	MC1456V .
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7428 . 28	74141 . 88	8094 . 40	4041 . 79	NE540L .
7430 . 21	74145 . 70	9095 . 67	4042 . 79	NE555V .
7432 . 25	74147 . 1.63	8096 . 67	4043 . 70	NE566A .
7433 . 30	74148 . 1.30	8097 . 67	4044 . 70	NE560B .
7437 . 25	74150 . 1.16	8098 . 67	4045 . 1.86	NE561B .
7438 . 25	74151 . 70	75150 . 1.16	4049 . 40	NE562B .
7440 . 21	74153 . 65	75450 . 88	4050 . 40	NE565A .
7442 . 53	74154 . 103	75451 . 61	4051 . 1.26	NE566V .
7443 . 63	74155 . 70	75452 . 61	4052 . 1.26	NE567V .
7445 . 70	74156 . 70	75453 . 61	4053 . 1.26	uA709CV .
7446 . 70	74157 . 70	75454 . 61	4060 . 1.58	uA710CA .
7447 . 70	74160 . 88	75455 . 81	4066 . 79	uA711CA .
7448 . 70	74161 . 88	75456 . 84	4070 . 23	uA712CA .
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7454 . 21	74165 . 115	4001 . 23	4081 . 23	uA748CV .
7459 . 21	74166 . 126	4002 . 23	4082 . 23	uA7805CU .
7460 . 21	74167 . 264	4003 . 23	4502 . 79	uA7806CU .
7470 . 30	74170 . 96	4004 . 23	4503 . 79	uA7808CU .
7472 . 30	74174 . 98	4007 . 23	4511 . 105	uA7812CU .
7473 . 30	74175 . 93	4008 . 79	4514 . 2.80	uA7815CU .
7474 . 30	74176 . 79	4009 . 79	4515 . 2.80	uA7818CU .
7475 . 49	74177 . 79	4010 . 1.23	4516 . 1.14	uA7824CU .
	74180 . 70	4011 . 23		

BASIC Algorithms for Common Math Functions

By Michael P. Burton (BAFCMF)

Some smaller versions of BASIC utilize standard floating point arithmetic but do not contain the commonly used math functions sine, cosine, e^x , $\log e$ and square root. All of these functions except square root can be expressed as series, which are easily converted to algorithms written in BASIC. For the square root function, there is an approximation method which can also be written as a BASIC algorithm. The following routines are the algorithms for $\sin(x)$, $\cos(x)$, $\exp(x)$, $\ln(x)$ and \sqrt{x} . Please note the constraints placed on the values of x . Within the given boundaries of x , the routines are accurate to seven digits.

The following BASIC program was developed for SWTP's 6800 Microcomputer and runs on the SWTP's standard 4K BASIC Interpreter version 2.0 with floating point.

INTERFACE EQUIPMENT: SWTPC CT1024 with SWTPC's AC-30 Cassette Interface.

SEE MICROCOMPUTER SOFTWARE DEPOSITORY PROGRAM INDEX FOR COPIES OF THIS PROGRAM

BASIC ALGORITHMS FOR COMMON MATH FUNCTIONS

SYMBOLIC NAME: BAFCMF

PROGRAMMER: MICHAEL P. BURTON

MICROCOMPUTER: SWTPC 6800

INTERFACE EQUIPMENT: SWTPC CT1024 WITH AC-30 CASSETTE INTERFACE

SUPPORT SOFTWARE: SWTPC 4K BASIC

```

1000 REM SIN ALGORITHM
1005 REM X=INPUT ANGLE EXPRESSED IN DEGREES
1010 REM X1=RESULT (X1=SIN(X))
1015 REM -180.0<=X<=180.0
1020 LET N1=1
1025 LET N2=-1
1030 LET X1=0.0
1035 LET X2=1.0
1040 LET X3=X*(3.14159265/180.0)
1045 IF X>=(-180.0) THEN IF X<=180.0 THEN 1055
1050 PRINT "SIN BOUND ERR"
1055 FOR N=1 TO 15
1060 LET N1=N1*N
1065 LET X2=X2*X3
1070 IF N=(INT(N/2)*2) THEN 1085
1075 LET N2=INT(N2*(-1))
1080 LET X1=X1+(X2*INT(N2))/(INT(N1))
1085 NEXT N
1090 RETURN
1100 REM COSINE ALGORITHM
1105 REM X=INPUT ANGLE EXPRESSED IN DEGREES
1110 REM X1=RESULT (X1=COS(X))
1115 REM -180.0<=X<=180.0
1120 LET N1=1
1125 LET N2=1
1130 LET X1=1.0
1135 LET X3=X*(3.14159265/180.0)
1140 LET X2=X3
1145 IF X>=(-180.0) THEN IF X<=180.0 THEN 1155
1150 PRINT "COS BOUND ERR"
1155 FOR N=2 TO 16
1160 LET N1=N1*N
1165 LET X2=X2*X3
1170 IF N<>(INT(N/2)*2) THEN 1185
1175 LET N2=INT(N2*(-1))
1180 LET X1=X1+(X2*INT(N2))/(INT(N1))
1185 NEXT N
1190 RETURN
1200 REM EXPONENTIAL ALGORITHM

```

```

1205 REM X=EXPONENT OF E
1210 REM X1=RESULT (X1=EXP(X))
1215 REM -5.0<=X<=22.0
1220 LET N1=1
1225 LET X1=1.0
1230 LET X2=1.0
1235 IF X>=(-5.0) THEN IF X<=22.0 THEN 1245
1240 PRINT "EXP BOUND ERR"
1245 FOR N=1 TO 51
1250 LET N1=N1*N
1255 LET X2=X2*X
1260 LET X1=X1+X2/(INT(N1))
1265 NEXT N
1270 RETURN
1300 REM LOGARITHM ROUTINE
1305 REM X1=LN(X)
1310 REM 0.1<=X<=10.0
1315 LET X1=0.0
1320 LET X2=1.0
1325 IF X>=0.1 THEN IF X<=10.0 THEN 1335
1330 PRINT "LN BOUND ERR"
1335 FOR N=1 TO 51
1340 LET X2=X2*((X-1.0)/(X+1.0))
1345 IF N=(INT(N/2)*2) THEN 1355
1350 LET X1=X1+X2/INT(N)
1355 NEXT N
1360 LET X1=2.0*X1
1365 RETURN
1400 REM SQUARE ROOT ALGORITHM
1405 REM X=INPUT VALUE
1410 REM X1=RESULT (X1=SQRT(X))
1415 REM X>0.0
1420 IF X>0.0 THEN 1435
1425 PRINT "SQRT BOUND ERROR"
1430 RETURN
1435 LET X1=X/2.0
1437 LET X3=0
1440 LET X2=(X/X1-X1)/2
1445 IF X2=0.0 THEN RETURN
1450 IF X2=X3 THEN RETURN
1455 LET X1=X1+X2
1457 LET X3=X2
1460 GOTO 1440
9999 END

```

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BASIC FLOATING POINT MATH PACKAGE

Part 3 of LLL 8080 Basic Interpreter Program

By David Mead

and modified by Hal Brand and Frank Olken

INTRODUCTION

This article is Part 3 of a series of four articles covering the LLL 8080 BASIC Interpreter program released to the public domain by Lawrence Livermore Laboratories. It includes the BASIC Floating Point Math Package assembly listing.

[illegible]

MICROCOMPUTER DEVELOPMENT SOFTWARE

INTERFACE AGE 105

MICROCOMPUTER DEVELOPMENT SOFTWARE

FEBRUARY 1977


```

0C79 CD 79 0C      CSIGN:  CALL      MSFH      :SET A=SIGN(H,L), E=SIGN(H,B
0C6C AB              XRA      ESTR      :INCLUDE OF OR SIGNS TO GET N
0C6D CD 71 0C      CALL      ESTR      :STORE SIGN INTO RESULT
0C70 C9              RET       :RETURN

:
:
:
SUBROUTINE CSTR
STORES VALUE IN A IN
CSTR?2
PUTS LPTP IN E
:
:
0C71 5D      CSTR:  MOV E,L      :SAVE LPTP IN E
0C72 69      MOV L,L      :CPTP TO L
0C73 2C      INR L        :LPTP?2
0C74 2C      INR L        :TO L
0C75 2C      INR L        :LPTP
0C76 77      MOV M,A      :STORE ANSWER
0C77 6A      MOV L,E      :LPTP BACK TO L
0C78 C9      RET

:
:
SUBROUTINE MSFH

THIS SUBROUTINE FETCHES THE SIGNS OF THE MANTISSA
OF THE FLOATING POINT NUMBERS POINTED TO BY (H,L)
AND (H,B) INTO THE A AND E REGISTERS RESPECTIVELY

REGISTERS ON EXIT:

A = SIGN OF MANTISSA OF (H,L)
E = SIGN OF (H,B)
B,C,D,H,L = SAME AS ON ENTRY

:
:
0C79 MSFH:  MOV E,L      :SAVE LPTP
0C7A 6D      MOV L,B      :BPTP TO L
0C7B 2C      INR L        :LPTP?2
0C7C 2C      INR L        :LPTP
0C7D 7E      MOV A,M      :BPTP?2 TO A
0C7E F6 B0   ANI 12B      :SAVE MANT SIGN
0C81 6A      MOV L,E      :LPTP BACK TO L
0C82 6A      MOV M,A      :STORE BPTP MANT SIGN
0C83 2C      INR L        :LPTP?2
0C84 2C      INR L        :TO L
0C85 2C      INR L        :LPTP
0C86 7E      MOV A,M      :LPTP?2 TO A
0C87 1B      ANI 12B      :SAVE LPTP MANT SIGN
0C88 2D      DCR L        :LPTP BACK
0C89 2D      DCR L        :TO L
0C8A 2D      DCR L        :LPTP
0C8B C9      RET
0C8C

:
:
SUBROUTINE OCTL
MOVPS RPTP CHAR TO LPTP CHAP
DESTROYSE
:
:
0C8D OCTL:  MOV E,L      :BPTP TO E
0C8E 6D      MOV L,B      :BPTP TO L
0C8F 2C      INR L        :LPTP?2
0C90 2C      INR L        :LPTP
0C91 2C      INR L        :TO L
0C92 7E      MOV A,M      :BPTP CHAP TO A
0C93 6A      MOV L,E      :LPTP TO L
0C94 2C      INR L        :LPTP?2
0C95 2C      INR L        :TO L
0C96 2C      INR L        :LPTP
0C97 77      MOV M,A      :STORE RPTP CHAP IN LPTP CHAP
0C98 6A      MOV L,E      :LPTP TO L
0C99 C9      RET

```

```
*****ROUTINE TO CONVERT FLOATING PT. OUTPUT
*****CALLED OVER - NOTE: THIS IS CURRENTLY SET
*****TO OUTPUT ROUTINE
```

```

0000 C0 0A 0A          CALL ZCHK          ;CHECK FOR NEW ZERO
0001 C2 B2 JC          JNZ NZC10          ;NEW ZERO
0002 0C              INR C              ;INCR C
0003 0C              MOV L,C           ;L=C
0004 C2 80 BU          CALL MZEP          ;MOVE TO DECIMAL EXPONENT
0005 2C              INR L              ;INCR L
0006 C2 0C              INR L              ;INCR L
0007 2C              INR L              ;INCR L
0008 C2 0C              INR L              ;INCR L
0009 AF              XRA A              ;XOR A
000A 77              MOV M,A           ;MOVE M=A
000B C0 93 3D          JMC SIGN          ;WRITE OUT SIGN
000C AF 11 0D          JMD M           ;OUTPUT 1
000D 36              NNZPD:           ;IF SET THE NUMBER TO COUNT
000E 2C              INR L              ;INCR L
000F 46 25            MOV B,M           ;MOV B,M
0010 2C              INR L              ;INCR L
0011 4E 25            MOV E,M           ;MOV E,M
0012 7E              INR L              ;INCR L
0013 4E 25            MOV A,M           ;MOVE A=M
0014 0C              INR C              ;INCR C
0015 0C              INR C              ;INCR C
0016 0C              INR C              ;INCR C
0017 46 25            MOV L,C           ;MOVE L=C
0018 72              MOV M,D           ;MOVE M=D
0019 2C              INR L              ;INCR L
001A 72              MOV M,B           ;MOVE M=B
001B 2C              INR L              ;INCR L
001C 72              MOV M,F           ;MOVE M=F
001D 2C              INR L              ;INCR L
001E 46 25            MOV B,A           ;MOV B=A
001F 4E 25            MOV A,M           ;MOVE A=M
0020 C3 06 F7          ANI 1770         ;ANI 1770
0021 46 25            MOV M,A           ;MOVE M=A
0022 C3 10 00          CPI 1700         ;CPI 1700
0023 2C              JZ NZRD           ;JZ NZRD
0024 0C              INR L              ;INCR L
0025 72              RLC              ;RLC
0026 2C              INR L              ;INCR L
0027 46 25            MOV M,A           ;MOVE M=A
0028 72              MOV M,B           ;MOVE M=B
0029 2C              INR L              ;INCR L
002A 72              MOV M,A           ;MOVE M=A
002B 2C              INR L              ;INCR L
002C 78 33            CALL SIGN          ;CALL SIGN
002D 2C              INR L              ;INCR L
002E 17 33            MVI L,(17ENS AND 3770) ;MVI L,(17ENS AND 3770)
002F C3 F4 0D          CALL CCPT          ;CALL CCPT
0030 C3 F4 3D          CALL GCHR          ;CALL GCHR
0031 46 25            MOV B,A           ;MOV B=A
0032 46 10 3C          ANI 103C         ;ANI 103C
0033 46 25            MOV M,B           ;MOVE M=B
0034 72              RLC              ;RLC
0035 72              MOV M,B           ;MOVE M=B
0036 C3 06 0C          JZ GDTV          ;JZ GDTV
0037 46 83            MVI A,-2700      ;MVI A=-2700
0038 46 25            MOV M,A           ;MOVE M=A
0039 0C              INR C              ;INCR C
003A 72              MOV M,B           ;MOVE M=B
003B 72              MOV M,B           ;MOVE M=B
003C 72              MOV M,B           ;MOVE M=B
003D 72              MOV M,B           ;MOVE M=B
003E 72              MOV M,B           ;MOVE M=B
003F 72              MOV M,B           ;MOVE M=B
0040 72              MOV M,B           ;MOVE M=B
0041 72              MOV M,B           ;MOVE M=B
0042 72              MOV M,B           ;MOVE M=B
0043 72              MOV M,B           ;MOVE M=B
0044 72              MOV M,B           ;MOVE M=B
0045 72              MOV M,B           ;MOVE M=B
0046 72              MOV M,B           ;MOVE M=B
0047 72              MOV M,B           ;MOVE M=B
0048 72              MOV M,B           ;MOVE M=B
0049 72              MOV M,B           ;MOVE M=B
004A 72              MOV M,B           ;MOVE M=B
004B 72              MOV M,B           ;MOVE M=B
004C 72              MOV M,B           ;MOVE M=B
004D 72              MOV M,B           ;MOVE M=B
004E 72              MOV M,B           ;MOVE M=B
004F 72              MOV M,B           ;MOVE M=B
0050 72              MOV M,B           ;MOVE M=B
0051 72              MOV M,B           ;MOVE M=B
0052 72              MOV M,B           ;MOVE M=B
0053 72              MOV M,B           ;MOVE M=B
0054 72              MOV M,B           ;MOVE M=B
0055 72              MOV M,B           ;MOVE M=B
0056 72              MOV M,B           ;MOVE M=B
0057 72              MOV M,B           ;MOVE M=B
0058 72              MOV M,B           ;MOVE M=B
0059 72              MOV M,B           ;MOVE M=B
005A 72              MOV M,B           ;MOVE M=B
005B 72              MOV M,B           ;MOVE M=B
005C 72              MOV M,B           ;MOVE M=B
005D 72              MOV M,B           ;MOVE M=B
005E 72              MOV M,B           ;MOVE M=B
005F 72              MOV M,B           ;MOVE M=B
0060 72              MOV M,B           ;MOVE M=B
0061 72              MOV M,B           ;MOVE M=B
0062 72              MOV M,B           ;MOVE M=B
0063 72              MOV M,B           ;MOVE M=B
0064 72              MOV M,B           ;MOVE M=B
0065 72              MOV M,B           ;MOVE M=B
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006A 72              MOV M,B           ;MOVE M=B
006B 72              MOV M,B           ;MOVE M=B
006C 72              MOV M,B           ;MOVE M=B
006D 72              MOV M,B           ;MOVE M=B
006E 72              MOV M,B           ;MOVE M=B
006F 72              MOV M,B           ;MOVE M=B
0070 72              MOV M,B           ;MOVE M=B
0071 72              MOV M,B           ;MOVE M=B
0072 72              MOV M,B           ;MOVE M=B
0073 72              MOV M,B           ;MOVE M=B
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0078 72              MOV M,B           ;MOVE M=B
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007A 72              MOV M,B           ;MOVE M=B
007B 72              MOV M,B           ;MOVE M=B
007C 72              MOV M,B           ;MOVE M=B
007D 72              MOV M,B           ;MOVE M=B
007E 72              MOV M,B           ;MOVE M=B
007F 72              MOV M,B           ;MOVE M=B
0080 72              MOV M,B           ;MOVE M=B
0081 72              MOV M,B           ;MOVE M=B
0082 72              MOV M,B           ;MOVE M=B
0083 72              MOV M,B           ;MOVE M=B
0084 72              MOV M,B           ;MOVE M=B
0085 72              MOV M,B           ;MOVE M=B
0086 72              MOV M,B           ;MOVE M=B
0087 72              MOV M,B           ;MOVE M=B
0088 72              MOV M,B           ;MOVE M=B
0089 72              MOV M,B           ;MOVE M=B
008A 72              MOV M,B           ;MOVE M=B
008B 72              MOV M,B           ;MOVE M=B
008C 72              MOV M,B           ;MOVE M=B
008D 72              MOV M,B           ;MOVE M=B
008E 72              MOV M,B           ;MOVE M=B
008F 72              MOV M,B           ;MOVE M=B
0090 72              MOV M,B           ;MOVE M=B
0091 72              MOV M,B           ;MOVE M=B
0092 72              MOV M,B           ;MOVE M=B
0093 72              MOV M,B           ;MOVE M=B
0094 72              MOV M,B           ;MOVE M=B
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0096 72              MOV M,B           ;MOVE M=B
0097 72              MOV M,B           ;MOVE M=B
0098 72              MOV M,B           ;MOVE M=B
0099 72              MOV M,B           ;MOVE M=B
009A 72              MOV M,B           ;MOVE M=B
009B 72              MOV M,B           ;MOVE M=B
009C 72              MOV M,B           ;MOVE M=B
009D 72              MOV M,B           ;MOVE M=B
009E 72              MOV M,B           ;MOVE M=B
009F 72              MOV M,B           ;MOVE M=B
00A0 72              MOV M,B           ;MOVE M=B
00A1 72              MOV M,B           ;MOVE M=B
00A2 72              MOV M,B           ;MOVE M=B
00A3 72              MOV M,B           ;MOVE M=B
00A4 72              MOV M,B           ;MOVE M=B
00A5 72              MOV M,B           ;MOVE M=B
00A6 72              MOV M,B           ;MOVE M=B
00A7 72              MOV M,B           ;MOVE M=B
00A8 72              MOV M,B           ;MOVE M=B
00A9 72              MOV M,B           ;MOVE M=B
00AA 72              MOV M,B           ;MOVE M=B
00AB 72              MOV M,B           ;MOVE M=B
00AC 72              MOV M,B           ;MOVE M=B
00AD 72              MOV M,B           ;MOVE M=B
00AE 72              MOV M,B           ;MOVE M=B
00AF 72              MOV M,B           ;MOVE M=B
00B0 72              MOV M,B           ;MOVE M=B
00B1 72              MOV M,B           ;MOVE M=B
00B2 72              MOV M,B           ;MOVE M=B
00B3 72              MOV M,B           ;MOVE M=B
00B4 72              MOV M,B           ;MOVE M=B
00B5 72              MOV M,B           ;MOVE M=B
00B6 72              MOV M,B           ;MOVE M=B
00B7 72              MOV M,B           ;MOVE M=B
00B8 72              MOV M,B           ;MOVE M=B
00B9 72              MOV M,B           ;MOVE M=B
00BA 72              MOV M,B           ;MOVE M=B
00BB 72              MOV M,B           ;MOVE M=B
00BC 72              MOV M,B           ;MOVE M=B
00BD 72              MOV M,B           ;MOVE M=B
00BE 72              MOV M,B           ;MOVE M=B
00BF 72              MOV M,B           ;MOVE M=B
00C0 72              MOV M,B           ;MOVE M=B
00C1 72              MOV M,B           ;MOVE M=B
00C2 72              MOV M,B           ;MOVE M=B
00C3 72              MOV M,B           ;MOVE M=B
00C4 72              MOV M,B           ;MOVE M=B
00C5 72              MOV M,B           ;MOVE M=B
00C6 72              MOV M,B           ;MOVE M=B
00C7 72              MOV M,B           ;MOVE M=B
00C8 72              MOV M,B           ;MOVE M=B
00C9 72              MOV M,B           ;MOVE M=B
00CA 72              MOV M,B           ;MOVE M=B
00CB 72              MOV M,B           ;MOVE M=B
00CC 72              MOV M,B           ;MOVE M=B
00CD 72              MOV M,B           ;MOVE M=B
00CE 72              MOV M,B           ;MOVE M=B
00CF 72              MOV M,B           ;MOVE M=B
00D0 72              MOV M,B           ;MOVE M=B
00D1 72              MOV M,B           ;MOVE M=B
00D2 72              MOV M,B           ;MOVE M=B
00D3 72              MOV M,B           ;MOVE M=B
00D4 72              MOV M,B           ;MOVE M=B
00D5 72              MOV M,B           ;MOVE M=B
00D6 72              MOV M,B           ;MOVE M=B
00D7 72              MOV M,B           ;MOVE M=B
00D8 72              MOV M,B           ;MOVE M=B
00D9 72              MOV M,B           ;MOVE M=B
00DA 72              MOV M,B           ;MOVE M=B
00DB 72              MOV M,B           ;MOVE M=B
00DC 72              MOV M,B           ;MOVE M=B
00DD 72              MOV M,B           ;MOVE M=B
00DE 72              MOV M,B           ;MOVE M=B
00DF 72              MOV M,B           ;MOVE M=B
00E0 72              MOV M,B           ;MOVE M=B
00E1 72              MOV M,B           ;MOVE M=B
00E2 72              MOV M,B           ;MOVE M=B
00E3 72              MOV M,B           ;MOVE M=B
00E4 72              MOV M,B           ;MOVE M=B
00E5 72              MOV M,B           ;MOVE M=B
00E6 72              MOV M,B           ;MOVE M=B
00E7 72              MOV M,B           ;MOVE M=B
00E8 72              MOV M,B           ;MOVE M=B
00E9
```

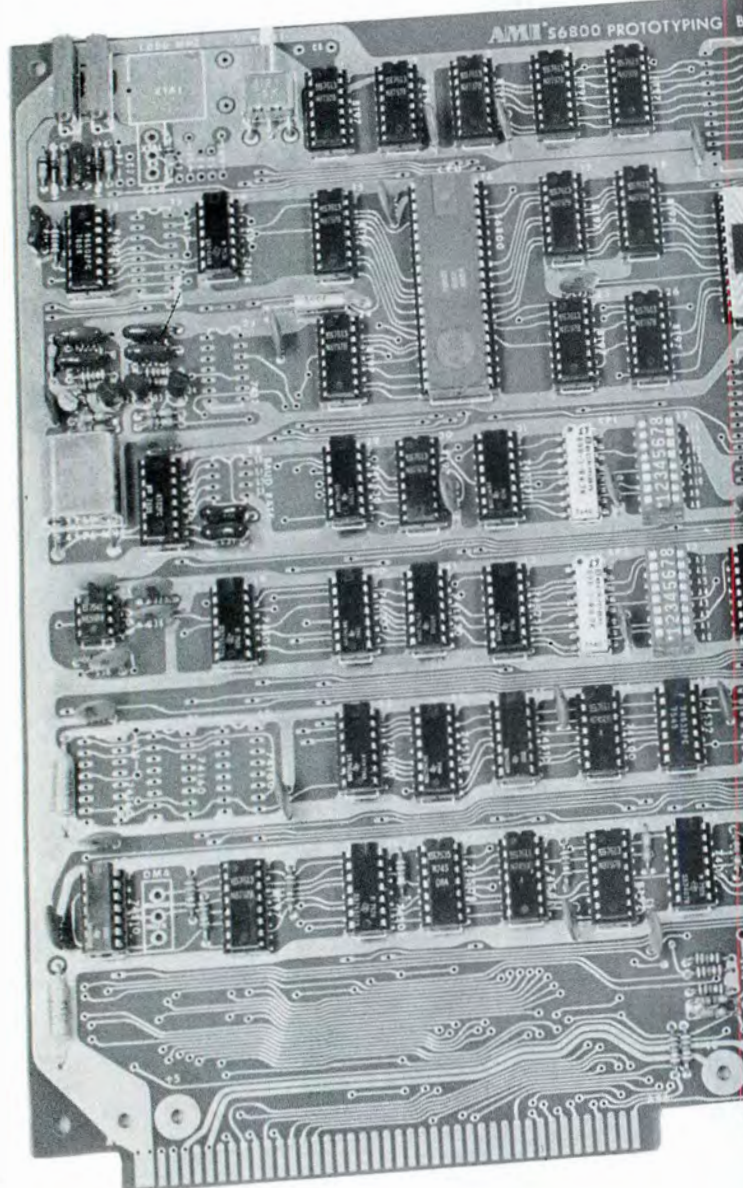
```

0051 C9 RET ;SERVES AS TERM FOR DIOG & C
0052 1E 01 MVI E,1 ;MULT. BY 10 (START WITH X2)
0053 7F 30 CALL L5FT ;MULT. SHIFT L = X2
0054 69 MOV L,C ;SAVE X2 IN "RESULT"
0055 2D MCR L ;SET TO TOP OF NUMBER
0056 2D MCR L ;SET C TO RESULT
0057 69 MOV A,C
0058 4F ADD 110 ;/MOD C SET RIGHT
0059 2C 09 MOV A,M ;/MOD RTR FOD RAM TRANSFER
0060 02 0F CALL COPY ;/SAVE X2 FINALLY
0061 79 MOV A,L ;/MULT RESET
0062 09 SUI 1 ;/BACK TO NORMAL
0063 4E MOV A,M
0064 1E 02 MOV A,C ;/MOD GET 1X21X4=X8
0065 2C MOV A,C ;/BUT MUST SAVE OVERFLOW
0066 2D DCR L
0067 69 7D 0D CALL TLP2 ;/GET X8
0068 2C MOV L,C ;/SET UP TO CALL QAND
0069 79 MOV A,C ;/SET R TO X2
0070 0A 47 TLOP X2 ;/TO X2
0071 C3 36 38 CALL QAND ;/ADD TWO LOW WORDS
0072 2D DCR L ;/BACK UP TO OVERFLOW
0073 7F MOV A,M ;/MOD SET TC X2 OVERFLOW
0074 6E DCR L ;/ITS AT 81
0075 8E ADC H ;/ADD WITH CARRY - CARRY WAS P
0076 C9 RET ;/ALL DONE, RETURN OVERFLOW IN
0077 2C 09 L5FT: MOV A,C ;/SET PTR FOD LEFT SHIFT OF NU
0078 2C 09 MCR L ;/BACK UP TO OVERFLOW
0079 4F XRA A ;/OVERFLOW=0 1ST TIME
0080 7F TLOP: MOV M,A ;/SAVE OVERFLOW
0081 2C DCR E ;/TEST FOR DONE
0082 7F RM ;/DONE WHEN E MINUS
0083 2C INR L ;/MOVE TO LOW
0084 2C INR L ;/**** EXTENSION
0085 17 RAL ;/SHIFT LEFT 4 BYTES
0086 2C MOV A,M ;/PUT BACK
0087 79 DCR L ;/**** - ALL DONE
0088 2C MOV A,M ;/GET LOW
0089 7F RAL ;/SHIFT LEFT 1
0090 7F MOV A,M ;/RESTORE IT
0091 2C DCR L ;/BACK UP TO HIGH
0092 7F MOV A,M ;/GET HIGH
0093 17 RAL ;/SHIFT IT LEFT WITH CARRY
0094 2C MOV A,M ;/PUT IT BACK
0095 7F DCR L ;/BACK UP TO OVERFLOW
0096 2C MOV A,M ;/GET OVERFLOW
0097 7F RAL ;/SHIFT IT LEFT
0098 2C JNC TLOP ;/GO FOR MORE
0099 E6 80 SIGN: ANI 2000 ;/GET SIGN BIT
0100 93 90 JC PL5V ;/TEST FOR INSTAD OF PLUS
0101 3E 0D JZ PL5V ;/TEST FOR -
0102 3E 0F MVI A,2550 ;/NEGATIVE
0103 2C CALL OUTR ;/OUTPUT SIGN
0104 69 GCHP: MOV L,C ;/GET CHARACTERISTIC
0105 2C GETA: INR L ;/MOVE TO IT
0106 2C INR L ;/****
0107 2C INR L ;/GETTC INTO A
0108 2C RET ;/OCNE
0109 C1 0D MORD: CALL GETEX ;/MUL OR DIV DEPENDING ON EXP
0110 45 MOV E,A ;/SAVE DECIMAL EXP
0111 2C MOV B,L ;/SET UP TO MULT OR DIV
0112 69 INR B ;/INR BOP POINTINT SET
0113 2C MOV L,C ;/L POINTS TO NUMBER TO CONVP
0114 2D ADD 110 ;/POINT C AT "RESULT" AREA
0115 2C MOV A,C ;/IN SCPTCH
0116 2C MOV A,M ;/MOD C SET RIGHT
0117 7F MVI A,200 ;/NOW TEST FOR MUL
0118 2C JNC TEST ;/TEST NEGATIVE DEC. EXP.
0119 7F JZ DIVIT ;/IF EXP IS + THEN DIVIDE
0120 2C CALL LMUL ;/MULT.
0121 79 FINUP: MOV A,C ;/SAVE LOC. CF RESULT
0122 2C MOV C,L ;/LOC OF NUMBER IT WAS DESI
0123 2C MOV A,L ;/SET L TO LOC. OF RESULT
0124 2C MOV A,M ;/SHOOW RAM TO RAM RAM
0125 2C CALL COPY ;/MOVE RESULT TO NUMBER
0126 2C MOV L,C ;/NOW GET DECIMAL EXP
0127 2C INR L ;/****
0128 C1 0D DIVIT: JMP GETA ;/USE PART OF GCHP
0129 2C CALL LOV ;/DIVIDF
0130 2C JMP FINUP ;/****
0131 E3 0D TMOO: CALL CTMO ;/CONVERT TO 2 DIGITS
0132 2C MOV B,A ;/SAVE ONES DIGIT
0133 2C CALL GETEX ;/GET DECIMAL EXP
0134 2C MOV E,A ;/SAVE A COPY
0135 2C ANI 220 ;/SET FOR NEGATIVE
0136 2C JZ ADD1 ;/BUMP EXP BY 1 SINCE 2 DIGITS
0137 2C DCP E ;/DECREMENT NEGATIVE EXP SINCE
0138 2C MOV A,B ;/RESTORE EXP WITH NEW VALUE
0139 2C JNP INPD ;/NOW DO 2ND DIGIT
0140 C3 25 0D FINIT: JNC OUT2 ;/GO OUT 2ND AND REST FOR DIGIT
0141 2C INR L ;/COMPENSATE FOR 2 DIGITS
0142 E0 0D C2ND: MOV FINIT ;/CONVERT 2 DIGIT BIN TO BCD
0143 1E FF LMOO: INR L ;/ADD UP TENS DIGIT
0144 2C SUI 120 ;/SUBTRACT 10
0145 2C JPL 00P ;/TILL NEGATIVE RESULT
0146 2C ADD 120 ;/RESTORE ONES DIGIT
0147 2C MOV B,A ;/SAVE ONES DIGIT
0148 2C MOV A,E ;/GET TENS DIGIT
0149 C3 3D 0D OUT2: CALL DIGO ;/OUTPUT IT
0150 2C MOV A,B ;/SET A TO 2ND DIGIT
0151 2C RET ;/****
0152 69 COPT: MOV A,C ;/COPY FROM 137N TO 14M
0153 2C ADD 5 ;/SET C TO PLACE TO PUT
0154 2C MVI A,(TEN5/256) ;/COPY IT
0155 2C CALL COPY ;/NOW RESET C
0156 2C SUI 5 ;/ITS RESET
0157 2C MOV C,A ;/****
0158 2C COPY: MOV B,M ;/SAVE RAM H
0159 2C MOV A,B ;/SET TO DESTINATION RAM
0160 2C MOV A,P ;/GET A WORDS H
0161 2C INR L ;/LEFT & WORDS INTO THE REGS.
0162 2C MOV D,M ;/****
0163 2C INR L ;/****
0164 2C INP ;/****
0165 2C MOV L,M ;/****
0166 2C MOV A,B ;/****
0167 2C MOV B,L ;/****
0168 2C MOV L,C ;/****
0169 2C MOV A,M ;/****
0170 2C INR L ;/****
0171 2C MOV A,M ;/****
0172 2C MOV M,D ;/****
0173 2C INR L ;/****
0174 2C MOV A,M ;/****
0175 2C MOV A,B ;/****
0176 C9 RET ;/ALL & COPIED NOW
0177 2C ;/ALL DONE
0178 2C ;/****
0179 2C ;/****
0180 2C ;/****
0181 2C ;/****
0182 2C ;/****
0183 2C ;/****
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0333 2C ;/****
0334 2C ;/****
0335 2C ;/****
03
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JE28	3C	INR C	BY 2	0ED4	FE	AD	CPI 2550	;/TEST FJR -
JE29	3D	CALL ZROIT	CALL ZRCP NUMBER	0ED5	JNZ TRYP	09	MOV L+C	;/NOT MINUS
JE30	77	MOV M+A	/DECIMAL EXPONENT	0ED6	INR L	2C	INR L	;/MINUS 50 SET SIGN
JE31	77	CALL GNUM	/GET INTEGER PART OF NUM	0ED7	INR L	2C	INR L	;/IN CHAR LOC.
JE32	77	CALL GNUM	/TERM-2	0ED8	INR L	2C	INR L	;/**TP
JE33	77	J2 DECTP	YES	0ED9	36	80	MOV M+2000	;/SET - SIGN
JE34	77	J2 INEXP	/YES - 4*HOLD EXP	0EDA	JMP GNUM	0E	TRYP:	;/IGNORE *
JE35	77	J2 INEXP	/TEST FJR SPACE TERM 1240R-26	0EDB	FE	AB	CPI 2530	;/STRIP ASCII
JE36	77	J2 INEXP	/NOT LEGAL TERM	0EDC	CA	80	J2 GNUM	;/RETURN IF TERM
JE37	77	J2 INEXP	/FLOAT # AND SIGN IT	0EDD	F8	0A	J2 2800	;/TEST FOR NUMBER
JE38	77	J2 INEXP	/GET DECIMAL EXP	0EDE	F8	0A	CPI 120	;/ILLEGAL
JE39	77	J2 INEXP	/GET GOOD BITS	0EDF	F8	0A	RM	;/SAVE DIGIT
JE40	77	J2 INEXP	/SAVE COPY	0EE0	F8	0A	RP	;/LOC OF DIGIT STORAGE TO L
JE41	77	J2 INEXP	/GET SIGN OF EXP	0EE1	F8	0A	MOV E+A	;/SAVE DIGIT
JE42	77	J2 INEXP	/INTO SIGN BIT	0EE2	F8	0A	CALL GETN	;/LOC OF DIGIT STORAGE TO L
JE43	77	J2 INEXP	/SET FLOPS	0EE3	F8	0A	MOV M+E	;/SAVE DIGIT
JE44	77	J2 INEXP	/SET FLOPS	0EE4	F8	0A	CALL MULT	;/MULT NUMBER BY 10
JE45	77	J2 INEXP	/SET FLOPS	0EE5	F8	0A	CALL MULT	;/TEST FOR TOO MANY DIGITS
JE46	77	J2 INEXP	/SET FLOPS	0EE6	F8	0A	RNZ	;/TOO MANY DIGITS
JE47	77	J2 INEXP	/SET FLOPS	0EE7	F8	0A	CALL GETN	;/GET DIGIT
JE48	77	J2 INEXP	/SET FLOPS	0EE8	F8	0A	MOV L+C	;/SET L TO NUMBER
JE49	77	J2 INEXP	/SET FLOPS	0EE9	F8	0A	INR L	;/**TP
JE50	77	J2 INEXP	/SET FLOPS	0EEA	F8	0A	INR L	;/ADD IN THE DIGIT
JE51	77	J2 INEXP	/SET FLOPS	0EEB	F8	0A	ADD M	;/PUT RESULT BACK
JE52	77	J2 INEXP	/SET FLOPS	0EEC	F8	0A	MOV M+A	;/NOW HIGH
JE53	77	J2 INEXP	/SET FLOPS	0EED	F8	0A	MOV M+A	;/GET HIGH TO ADD IN CARRY
JE54	77	J2 INEXP	/SET FLOPS	0EEF	F8	0A	ACT 00	;/ADD IN CARRY
JE55	77	J2 INEXP	/SET FLOPS	0EF0	F8	0A	MOV M+A	;/UPDATE HIGH
JE56	77	J2 INEXP	/SET FLOPS	0EF1	F8	0A	MOV M+A	;/**TP EXTENSION
JE57	77	J2 INEXP	/SET FLOPS	0EF2	F8	0A	MOV M+A	;/ADD IN CARRY
JE58	77	J2 INEXP	/SET FLOPS	0EF3	F8	0A	MOV M+A	;/**TP ALL DONE
JE59	77	J2 INEXP	/SET FLOPS	0EF4	F8	0A	MOV M+A	;/OVERFLOW ERROR
JE60	77	J2 INEXP	/SET FLOPS	0EF5	F8	0A	MOV M+A	;/BUMP DIGIT COUNT NOW
JE61	77	J2 INEXP	/SET FLOPS	0EF6	F8	0A	MOV M+A	;/GET DIGIT COUNT
JE62	77	J2 INEXP	/SET FLOPS	0EF7	F8	0A	MOV M+A	;/BUMP DIGIT COUNT
JE63	77	J2 INEXP	/SET FLOPS	0EF8	F8	0A	MOV M+A	;/UPDATE DIGIT COUNT
JE64	77	J2 INEXP	/SET FLOPS	0EF9	F8	0A	MOV M+A	;/GET NEXT CHAR
JE65	77	J2 INEXP	/SET FLOPS	0EFA	F8	0A	MOV M+A	;/MUST BE NUM. OR TERM
JE66	77	J2 INEXP	/SET FLOPS	0EFB	F8	0A	MOV M+A	;/POINT L AT NUMBER TO FLOAT
JE67	77	J2 INEXP	/SET FLOPS	0EFC	F8	0A	MOV M+A	;/GO FLOAT IT
JE68	77	J2 INEXP	/SET FLOPS	0EFD	F8	0A	MOV M+A	;/PUT NUMBER IN IL
JE69	77	J2 INEXP	/SET FLOPS	0EFE	F8	0A	MOV M+A	;/GET ADD OF L
JE70	77	J2 INEXP	/SET FLOPS	0EFF	F8	0A	MOV M+A	;/GET L OF RESULT
JE71	77	J2 INEXP	/SET FLOPS	0F00	F8	0A	MOV M+A	;/POINT L AT WORD TO SAVE C
JE72	77	J2 INEXP	/SET FLOPS	0F01	F8	0A	MOV M+A	;/SAVE C IN IL +1 SINCE IT W
JE73	77	J2 INEXP	/SET FLOPS	0F02	F8	0A	MOV M+A	;/SET UP TO CALL COPY
JE74	77	J2 INEXP	/SET FLOPS	0F03	F8	0A	MOV M+A	;/NOW LCC SET
JE75	77	J2 INEXP	/SET FLOPS	0F04	F8	0A	MOV M+A	;/FROM TO RAM COPY
JE76	77	J2 INEXP	/SET FLOPS	0F05	F8	0A	MOV M+A	;/COPY TO L
JE77	77	J2 INEXP	/SET FLOPS	0F06	F8	0A	MOV M+A	;/IL+1 RETURNED HERE SO SET A
JE78	77	J2 INEXP	/SET FLOPS	0F07	F8	0A	MOV M+A	;/NOW EVERYTHING HUNKY-DORRY
JE79	77	J2 INEXP	/SET FLOPS	0F08	F8	0A	MOV M+A	;/LAST LOC. IN SCATCH
JE80	77	J2 INEXP	/SET FLOPS	0F09	F8	0A	MOV M+A	;/PUT IN L
JE81	77	J2 INEXP	/SET FLOPS	0F0A	F8	0A	MOV M+A	;/GET DIGIT
JE82	77	J2 INEXP	/SET FLOPS	0F0B	F8	0A	MOV M+A	;/ZERO NUMBER
JE83	77	J2 INEXP	/SET FLOPS	0F0C	F8	0A	MOV M+A	;/**TP
JE84	77	J2 INEXP	/SET FLOPS	0F0D	F8	0A	MOV M+A	;/**TP
JE85	77	J2 INEXP	/SET FLOPS	0F0E	F8	0A	MOV M+A	;/**TP
JE86	77	J2 INEXP	/SET FLOPS	0F0F	F8	0A	MOV M+A	;/**TP
JE87	77	J2 INEXP	/SET FLOPS	0F10	F8	0A	MOV M+A	;/**TP
JE88	77	J2 INEXP	/SET FLOPS	0F11	F8	0A	MOV M+A	;/**TP
JE89	77	J2 INEXP	/SET FLOPS	0F12	F8	0A	MOV M+A	;/**TP
JE90	77	J2 INEXP	/SET FLOPS	0F13	F8	0A	MOV M+A	;/**TP
JE91	77	J2 INEXP	/SET FLOPS	0F14	F8	0A	MOV M+A	;/**TP
JE92	77	J2 INEXP	/SET FLOPS	0F15	F8	0A	MOV M+A	;/**TP
JE93	77	J2 INEXP	/SET FLOPS	0F16	F8	0A	MOV M+A	;/**TP
JE94	77	J2 INEXP	/SET FLOPS	0F17	F8	0A	MOV M+A	;/**TP
JE95	77	J2 INEXP	/SET FLOPS	0F18	F8	0A	MOV M+A	;/**TP
JE96	77	J2 INEXP	/SET FLOPS	0F19	F8	0A	MOV M+A	;/**TP
JE97	77	J2 INEXP	/SET FLOPS	0F1A	F8	0A	MOV M+A	;/**TP
JE98	77	J2 INEXP	/SET FLOPS	0F1B	F8	0A	MOV M+A	;/**TP
JE99	77	J2 INEXP	/SET FLOPS	0F1C	F8	0A	MOV M+A	;/**TP
JE00	77	J2 INEXP	/SET FLOPS	0F1D	F8	0A	MOV M+A	;/**TP
JE01	77	J2 INEXP	/SET FLOPS	0F1E	F8	0A	MOV M+A	;/**TP
JE02	77	J2 INEXP	/SET FLOPS	0F1F	F8	0A	MOV M+A	;/**TP
JE03	77	J2 INEXP	/SET FLOPS	0F20	F8	0A	MOV M+A	;/**TP
JE04	77	J2 INEXP	/SET FLOPS	0F21	F8	0A	MOV M+A	;/**TP
JE05	77	J2 INEXP	/SET FLOPS	0F22	F8	0A	MOV M+A	;/**TP
JE06	77	J2 INEXP	/SET FLOPS	0F23	F8	0A	MOV M+A	;/**TP
JE07	77	J2 INEXP	/SET FLOPS	0F24	F8	0A	MOV M+A	;/**TP
JE08	77	J2 INEXP	/SET FLOPS	0F25	F8	0A	MOV M+A	;/**TP
JE09	77	J2 INEXP	/SET FLOPS	0F26	F8	0A	MOV M+A	;/**TP
JE10	77	J2 INEXP	/SET FLOPS	0F27	F8	0A	MOV M+A	;/**TP
JE11	77	J2 INEXP	/SET FLOPS	0F28	F8	0A	MOV M+A	;/**TP
JE12	77	J2 INEXP	/SET FLOPS	0F29	F8	0A	MOV M+A	;/**TP
JE13	77	J2 INEXP	/SET FLOPS	0F2A	F8	0A	MOV M+A	;/**TP
JE14	77	J2 INEXP	/SET FLOPS	0F2B	F8	0A	MOV M+A	;/**TP
JE15	77	J2 INEXP	/SET FLOPS	0F2C	F8	0A	MOV M+A	;/**TP
JE16	77	J2 INEXP	/SET FLOPS	0F2D	F8	0A	MOV M+A	;/**TP
JE17	77	J2 INEXP	/SET FLOPS	0F2E	F8	0A	MOV M+A	;/**TP
JE18	77	J2 INEXP	/SET FLOPS	0F2F	F8	0A	MOV M+A	;/**TP
JE19	77	J2 INEXP	/SET FLOPS	0F30	F8	0A	MOV M+A	;/**TP
JE20	77	J2 INEXP	/SET FLOPS	0F31	F8	0A	MOV M+A	;/**TP
JE21	77	J2 INEXP	/SET FLOPS	0F32	F8	0A	MOV M+A	;/**TP
JE22	77	J2 INEXP	/SET FLOPS	0F33	F8	0A	MOV M+A	;/**TP
JE23	77	J2 INEXP	/SET FLOPS	0F34	F8	0A	MOV M+A	;/**TP
JE24	77	J2 INEXP	/SET FLOPS	0F35	F8	0A	MOV M+A	;/**TP
JE25	77	J2 INEXP	/SET FLOPS	0F36	F8	0A	MOV M+A	;/**TP
JE26	77	J2 INEXP	/SET FLOPS	0F37	F8	0A	MOV M+A	;/**TP
JE27	77	J2 INEXP	/SET FLOPS	0F38	F8	0A	MOV M+A	;/**TP
JE28	77	J2 INEXP	/SET FLOPS	0F39	F8	0A	MOV M+A	;/**TP
JE29	77	J2 INEXP	/SET FLOPS	0F3A	F8	0A	MOV M+A	;/**TP
JE30	77	J2 INEXP	/SET FLOPS	0F3B	F8	0A	MOV M+A	;/**TP
JE31	77	J2 INEXP	/SET FLOPS	0F3C	F8	0A	MOV M+A	;/**TP
JE32	77	J2 INEXP	/SET FLOPS	0F3D	F8	0A	MOV M+A	;/**TP
JE33	77	J2 INEXP	/SET FLOPS	0F3E	F8	0A	MOV M+A	;/**TP
JE34	77	J2 INEXP	/SET FLOPS	0F3F	F8	0A	MOV M+A	;/**TP
JE35	77	J2 INEXP	/SET FLOPS	0F40	F8	0A	MOV M+A	;/**TP
JE36	77	J2 INEXP	/SET FLOPS	0F41	F8	0A	MOV M+A	;/**TP
JE37	77	J2 INEXP	/SET FLOPS	0F42	F8	0A	MOV M+A	;/**TP
JE38	77	J2 INEXP	/SET FLOPS	0F43	F8	0A	MOV M+A	;/**TP
JE39	77	J2 INEXP	/SET FLOPS	0F44	F8	0A	MOV M+A	;/**TP
JE40	77	J2 INEXP	/SET FLOPS	0F45	F8	0A	MOV M+A	;/**TP
JE41	77	J2 INEXP	/SET FLOPS	0F46	F8	0A	MOV M+A	;/**TP
JE42	77	J2 INEXP	/SET FLOPS	0F47	F8	0A	MOV M+A	;/**TP
JE43	77	J2 INEXP	/SET FLOPS	0F48	F8	0A	MOV M+A	;/**TP
JE44	77	J2 INEXP	/SET FLOPS	0F49	F8	0A	MOV M+A	;/**TP
JE45	77	J2 INEXP	/SET FLOPS	0F4A	F8	0A	MOV M+A	;/**TP
JE46	77	J2 INEXP	/SET FLOPS	0F4B	F8	0A	MOV M+A	;/**TP
JE47	77	J2 INEXP	/SET FLOPS	0F4C	F8	0A	MOV M+A	;/**TP
JE48	77	J2 INEXP	/SET FLOPS	0F4D	F8	0A	MOV M+A	;/**TP
JE49	77	J2 INEXP	/SET FLOPS	0F4E	F8	0A	MOV M+A	;/**TP
JE50	77	J2 INEXP	/SET FLOPS	0F4F	F8	0A	MOV M+A	;/**TP
JE51	77	J2 INEXP	/SET FLOPS	0F50	F8	0A	MOV M+A	;/**TP
JE52	77	J2 INEXP	/SET FLOPS	0F51	F8	0A	MOV M+A	;/**TP
JE53	77	J2 INEXP	/SET FLOPS	0F52	F8	0A	MOV M+A	;/**TP
JE54	77	J2 INEXP	/SET FLOPS	0F53	F8	0A	MOV M+A	;/**TP
JE55	77	J2 INEXP	/SET FLOPS	0F54	F8	0A	MOV M+A	;/**TP
JE56	77	J2 INEXP	/SET FLOPS	0F55	F8	0A	MOV M+A	;/**TP
JE57	77	J2 INEXP	/SET FLOPS	0F56	F8	0A	MOV M+A	;/**TP
JE58	77	J2 INEXP	/SET FLOPS	0F57	F8	0A	MOV M+A	;/**TP
JE59	77	J2 INEXP	/SET FLOPS	0F58	F8	0A	MOV M+A	;/**TP
JE60	77	J2 INEXP	/SET FLOPS	0F59	F8	0A	MOV M+A	;/**TP
JE61	77	J2 INEXP	/SET FLOPS	0F5A	F8	0A	MOV M+A	;/**TP
JE62	77	J2 INEXP	/SET FLOPS	0F5B	F8	0A	MOV M+A	;/**TP
JE63	77	J2 INEXP	/SET FLOPS	0F5C	F8	0A	MOV M+A	;/**TP
JE64	77	J2 INEXP	/SET FLOPS	0F5D	F8	0A	MOV M+A	;/**TP
JE65	77	J2 INEXP	/SET FLOPS	0F5E	F8	0A	MOV M+A	;/**TP
JE66	77	J2 INEXP	/SET FLOPS	0F5F	F8	0A	MOV M+A	;/**TP
JE67	77	J2 INEXP	/SET FLOPS	0F60	F8	0A	MOV M+A	;/**TP
JE68	77	J2 INEXP	/SET FLOPS	0F61	F8	0A	MOV M+A	;/**TP
JE69	77	J2 INEXP	/SET FLOPS	0F62	F8	0A	MOV M+A	;/**TP
JE70	77	J2 INEXP	/SET FLOPS	0F63	F8	0A	MOV M+A	;/**TP
JE71	77	J2 INEXP	/SET FLOPS	0F64	F8	0A	MOV M+A	;/**TP
JE72	77	J2 INEXP	/SET FLOPS	0F65	F8	0A	MOV M+A	;/**TP
JE73	77	J2 INEXP	/SET FLOPS	0F66	F8	0A	MOV M+A	;/**TP
JE74	77	J2 INEXP	/SET FLOPS	0F67	F8	0A	MOV M+A	;/**TP
JE75	77	J2 INEXP	/SET FLOPS	0F68	F8	0A	MOV M+A	;/**TP
JE76	77	J2 INEXP	/SET FLOPS	0F69	F8	0A	MOV M+A	;/**TP
JE77	77	J2 INEXP	/SET FLOPS	0F6A	F8	0A	MOV M+A	;/**TP
JE78	77	J2 INEXP	/SET FLOPS	0F6B	F8	0A	MOV M+A	;/**TP
JE79	77	J2 INEXP	/SET FLOPS	0F6C	F8	0A	MOV M+A	;/**TP
JE80	77	J2 INEXP	/SET FLOPS	0F6D	F8	0A	MOV M+A	;/**TP
JE81	77	J2 INEXP	/SET FLOPS	0F6E	F8	0A	MOV M+A	;/**TP
JE82	77	J2 INEXP	/SET FLOPS	0F6F	F8	0A	MOV M+A	;/**TP
JE83	77	J2 INEXP	/SET FLOPS	0F70	F8	0A	MOV M+A	;/**TP
JE84	77	J2 INEXP	/SET FLOPS	0F71	F8	0A	MOV M+A	;/**TP
JE85	77	J2 INEXP	/SET FLOPS	0F72	F8	0A	MOV M+A	;/**TP
JE86	77	J2 INEXP	/SET FLOPS	0F73	F8	0A	MOV M+A	;/**TP
JE87	77	J2 INEXP	/SET FLOPS	0F74	F8	0A	MOV M+A	;/**TP
JE88	77							

AMI's EVK SERIES MICROCOMPUTER PROTOTYPING BOARDS

By Robert A. Stevens



INTRODUCTION

This article is Part Three of a series on the EVK Microcomputer hardware, firmware and supporting software. This month's subject covers the ROM resident Prototyping TTY MONITOR Operating System, PROTO.

PROTO SOFTWARE

The resident PROTO software program includes the following commands:

- L LOAD HEX** paper tape program into RAM memory
- P PUNCH HEX** paper tape from memory
- S SET** (write) specified data string characters into consecutive memory locations
- D DISPLAY** (prints) in HEX to TTY contents of specified memory locations
- G GO TO** user program at specified address and execute
- R PRINTS** contents of MPU register (C, B, A, X, P & S) on TTY at time the user's program was last interrupted
- B BURN** (copies) the contents of specified memory into the EPROM in the programming socket
- V VERIFY** (compares) contents of specified memory with EPROM or ROM in the programming socket
- I INPUT** (copies) contents of the EPROM or ROM in the programming socket into specified RAM memory locations
- M MOVE** (copies) contents of memory block from specified location to designated RAM memory location
- E END** of transmission (EOT) character terminates the end of punch paper tape record and punches EOT on paper tape.

The commands will operate on a single character OP CODE plus address parameters from the TTY keyboard.

PROTO COMMAND DESCRIPTIONS

The EVK 300 board will be supplied with a prototyping operating system program (PROTO). The program resides in ROM with a starting address of F000. The various routines within PROTO are called by entering via the TTY keyboard one of the commands described in the following paragraphs. A command consists of one character command identifier followed by additional parameters, if needed, separated by blanks or commas. All commands end with a carriage

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return. Since no action is taken before the carriage return, an input line may be deleted by the use of the TTY ESCAPE key.

L, ADDL, ADDH, OFFSET

The Load tape command loads data from a hex formatted tape (see paragraph on 6800 HEX tape format at end of article) into the user's memory between ADDL and ADDH, inclusive. The OFFSET is added to the memory address specified on the tape to form the actual memory starting address for the data stored. If a byte to be stored into memory has an address outside of the range ADDL, ADDH, it is not entered into memory, but a Delete character (H'FF) is transmitted to the terminal.

Example: L 0100 02FF FFFA

The address range in the L command is optional, and if omitted is assumed to be the full range of memory (0000-FFFF). The offset parameter is also optional, and if omitted is assumed to be zero (0000). Thus the L command with no parameters loads the tape into the memory locations specified on the tape with no offset. The offset value in the L command is a two's complement signed number, entered in unsigned hexadecimal. For example, an offset of -6 is entered as FFFA.

If an attempt is made to load non-existent memory, or ROM, the loading operation will terminate, typing out the address and the message "BAD ADR."

In operating the Load command, PROTO turns on the tape reader and scans the tape for the first ASCII "S," which indicates start of record. It is not necessary to position the tape at the first record of a tape file since each record contains its own starting address.

PROTO will load data records until it encounters an end of file (EOF) record or a tape error (Check Sum or illegal character). When PROTO reads a header record (start of record and address), it translates the header into ASCII characters and prints the result. The Check Sum is the binary sum of all characters in the block.

PROTO does not list the tape contents as the tape is being read.

When PROTO encounters an end of file record or a tape error, it turns off the reader and prints "EOF" or "CKSM ERR" respectively.

P, ADDL, ADDH, OFFSET

The Punch hex format command causes PROTO to punch on the TTY paper tape the contents of memory between ADDL and ADDH, inclusive. Each record is

punched with a four-digit hex address of the starting byte of the record. This address is derived from the memory address of the byte being punched, plus the offset value, OFFSET. The offset is optional, and if omitted is assumed to be zero.

All data records are punched in hex format. Records using this command (except the last record) contain 16 bytes of data plus the start code, byte count, address, and the checksum.

The P command does not cause an EOF record to be punched so that several disjoint blocks of memory can be combined on one tape file.

Example: P F000 F07F 0F00

S, ADDR, BYTE1, BYTE2, ———, BYTEN

The Set memory command writes the 8-bit data words specified by BYTE1 to BYTEN into consecutive memory locations starting at ADD.

If ADD has more than 4 (hexadecimal) characters or if any of the data bytes have more than 2 characters each, only the last 4 or 2 characters are used respectively.

Example: S 0000 86 05 97 28

Memory locations at 0000 through 0003 are loaded as shown.

D, ADDL, ADDH

The Display memory command prints the contents of memory between ADDL and ADDH, inclusive, in hex format. Up to sixteen bytes per line are printed, preceded by the hexadecimal address of the first byte of the line. A carriage return is forced after a byte having a low order digit of F in its memory address is printed.

Example: D FC00 FC1F

Two lines of memory contents are printed as follows:

```
FC00 00 01 02 03 04 . . . 0E0F
FC10 10 11 12 13 14 . . . 1E1F
```

G, ADDR

The Go command starts execution of the user program at the address specified by the input parameter. To insure that all registers contain the same information they held before the user program was interrupted, PROTO pushes into the stack the copy of the user registers that it keeps at locations FFEB—FFF3 (CC, B, A, X, P, S) then executes an RTI instruction. The user can change the initial values of the

registers by changing the contents of these locations.

Example: G 300

Program will branch to address 0300 and start execution from that point.

R

The Registers command prints the contents of memory locations FFEF—FFF3 which contain the values that were in the user's C, B, A, X, P, and S registers (in that order) when the user's program was last interrupted.

B, ADDL, ADDH, ROMAD

The Burn command copies the contents of user memory into the EPROM in the programming socket, beginning with memory location ADDL through ADDH, inclusive, to EPROM locations beginning with address ROMAD. Each byte is burned in with 20 3-ms pulses of -50V on the V_{PROG} pin (pin 11) of the EPROM. Before attempting to write into the EPROM, the contents of the EPROM are compared with the user memory data byte to verify that the EPROM will take the byte (PROTO will not attempt to program a EPROM location to logic LOW which already contains logic HIGH). After the 20 pulses, the new contents of the EPROM are verified against the memory byte to be sure the data was indeed written. If the byte did not program, a NAK code is typed out on the terminal, and another try is made, up to a maximum of three tries.

If the preverify encounters a EPROM location containing HIGHs where the memory byte has zeros, PROTO will type out the memory address, the memory byte in binary, the EPROM byte in binary, and the EPROM address (if different from the memory address), then stop. If after attempting to write data into the EPROM, the data does not program, or erroneous bits show up, a similar display occurs for the failing location, with the additional message "BAD ADR" typed on the same line.

The EPROM address ROMAD is optional, and if omitted, ADDL is used, with only the least significant nine bits of the address being used. If the address range ADDL, ADDH is omitted, the 512 bytes beginning at FC00 are used, and the EPROM is checked to insure it contains all LOWs before any locations are written. If not, four question marks are typed and the B command is aborted.

V, ADDL, ADDH, ROMAD

The Verify command compares user memory between ADDL and ADDH, inclusive, with the corresponding locations in the EPROM in the programming socket, beginning with EPROM address ROMAD. Each location that does not match is typed out in the following format:

```
aaaa mmmmmmmmm pppppppp rrrr
```

where "aaaa" represents the user memory address, "mmmmmmmm" represents the memory byte, in binary, and "rrrr" represents the EPROM address, if different from the memory address (in the low nine bits). Nothing is typed for matching locations. The timeout may be aborted by typing an ESC key during

the timeout.

If the ROMAD parameter is omitted, ADDL is assumed. If no parameters are supplied in the command, the whole EPROM is compared to the contents of FC00 — FDFF.

I, ADDL, ADDH, ROMAD

The Input command copies the contents of an EPROM in the programming socket into memory beginning at the address ADDL through ADDH, inclusive, from the EPROM address ROMAD. If ROMAD is omitted, ADDL is assumed. If no parameters are supplied, the entire EPROM is copied into the RAM area, FC00 — FDFF. An attempt to copy an EPROM into non-existent memory will abort the command with the message "BAD ADR."

M, ADDL, ADDH, DEST

The Move command copies memory from the range ADDL — ADDH, inclusive, to the RAM locations starting at DEST. This copy begins at the lower address, so if DEST lies within the range ADDL — ADDH, some of the original data will be lost, and other parts will be duplicated.

E

The End of Transmission command is used to cause an EOT character to be punched on the paper tape. After a field has been punched, an EOT will terminate the record and punch a trailer tape. When reading a record, the reader will stop at the EOT character. If no EOT character is present, the reader must be manually turned off and the Reset switch must be pressed to enter the operating system program.

THE SUBROUTINE ROM

Many of the monitor's functions are accomplished with the help of the Re-Entrant Self-Relative Subroutine ROMs (RS)³. This standard ROM, which can be considered a software extension to the 6800 instruction set, is also available to be used by the user both on the prototype board and in his final production system. The user can call one of the 25 (RS)³ subroutines with an SWI instruction followed by the number of the desired subroutine.

The user should be aware of the fact that the (RS)³ pushes from 7 to 10 bytes of data onto the stack, depending upon which subroutines are called. This means that if the user calls (RS)³ routines, he must make sure that the necessary memory space is available for stack expansion.

Since PROTO assigns its own stack area, the user need not be concerned about how (RS)³ is used.

INTERRUPTS

Of the four available interrupt vectors, IRQ, RESET and SWI are used by PROTO while NMI is left for the user. The vectors are in RAM (except for RESET which is switch controlled) so the user writing his own program can completely control the system.

The upper memory locations are RAM. If the user

expects either NMI or IRQ interrupts to occur, he must initialize the vector addresses to the starting address of the IRQ and NMI handler routines.

PROTO must have control of the RESET vector so that the RESET switch on the Prototyping Board can return program control to PROTO at any time.

The reset routine copies the contents of the B, A, X, CC, and S registers into a fixed area of memory. This means that the program can be aborted at any time by using the reset switch while still saving all the registers except the program counter. Unfortunately, the contents of the program counter are lost.

It is possible for the user to use the NMI interrupt to abort a program execution without losing the contents of the P and C registers. This condition is automatically set in the NMI handling routine when PROTO is called. This interrupt vector will cause the contents of the user's registers to be printed when the NMI line goes low.

Since the SWI instruction is used to call sub-routines between 00 and H'18 from (RS)³ the user is somewhat limited in the ways he can use SWI instructions. However, he can access an SWI handler routine in his own program by an SWI instruction followed by a byte containing the decimal number less than H'80 but greater than H'19 $< n < \text{H}'80$ sequence, PROTO passes control at address FFF4. If the user expects to access his own SWI routine and use PROTO, he must use the Set Memory command to store the address of this routine at locations FFF4 and FFF5.

PROTO makes sure that the user's SWI routine is entered from the stack with all registers containing the same information that they would hold if the routine were entered directly through the SWI vector.

BREAKPOINTS

Breakpoints allow the user to halt his program and examine the contents of the internal registers. PROTO provides two types of breakpoints. In this system, breakpoints are actually debugging routines that can be called from the user's program just like (RS)³ routines.

Each breakpoint requires a two byte calling sequence: and SWI instruction followed by a number.

Breakpoints may be inserted either by reassembling the program with the extra SWI instructions added or the Set Memory command may be used to replace parts of the code with SWI instructions. Note that the second method is not satisfactory for the snapshot option (described below) since the replaced code must be restored before execution can be continued. When using the second method, the user must make sure that he replaces the first two bytes of an instruction. If the SWI replaces the second or third byte of an instruction, it may be interpreted as an address rather than an opcode.

The different types of breakpoints are:

1. Print registers (SWI, H'80)
2. Snapshot (SWI, H'81)

The sequence SWI, H'80 saves the user's registers at the vector stored in FFF4 — FFF5, prints their contents (in the order CC BB AA XXXX PPPP SSSS), then returns control to PROTO.

The sequence SWI, H'81 prints out the contents of

the user's registers then continues executing the user's program starting at the address following the byte containing the number H'81. Note that if this address does not contain a valid opcode, unpredictable results will occur.

6800 PAPER TAPE HEX FORMAT

The AMI 6800 Hex Tape format provides a compact representation of binary data patterns for transmission using ASCII communication terminals.

The Hex tape is organized into data records with each record containing information in the same format. The record information consists of type, length, address, data and checksum. All records begin with an 'S' character for start of record identification. All information on the tape which is not between a start of record and the checksum is ignored.

TAPE FORMAT

ASCII Character	Description
1	Start of record (S)
2	Type of record 0 — Header record 1 — Data record 9 — End of file record
3—4	Byte Count Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number

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- of characters to the end of the record. (This includes checksum and address data.)
- 5, 6, 7, 8 Address Value
The memory location where this record is to be stored.
- 9,...,N Data
Each data byte is represented by two hex characters.
- N+1, N+2 Checksum
The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

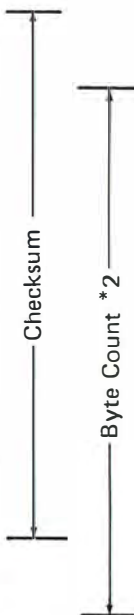
Example Data Record

Memory Contents

Address	Data
A000	10
A001	1A
A002	20
A003	2A

Data Record Contents

Character		Tape	
1	Start of record	53	S
2	Type of record	31	1
3	Byte count	30	0
4		37	7
5		41	A
6		30	0
7	Address	30	0
8		30	0
9	Data byte 1	31	1
10		30	0
11	Data byte 2	31	1
12		41	A
13	Data byte 3	32	2
14		30	0
15	Data byte 4	32	2
16		41	A
17	Checksum	38	8
18		34	4



The format for all hex tape records is diagrammed below.

Character	Header Record	Data Record	End-of-File Record
1	Start of Record	53	S
2	Type of Record	30	0
3	Byte Count	31	12
4		32	
5		30	
6	Address	30	0000
7	(if any)	30	
8		30	
9	Data	34	
10		38	
•		34	
•		34	
•		35	
•		32	
•			
•		41	
•		48	A8 (Checksum)
N	Checksum	39	
		45	9E

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PROGRAM INDEX FOR COPIES OF THIS PROGRAM.

PROTO PROGRAM

PAGE 1 PROTO 01/04/76 4122 PROTO

STMT	LOC	OBJECT	M	SOURCE STATEMENT	STMT	LOC	OBJECT	M	SOURCE STATEMENT
1				TITLE PROTO	146	0040	06 F8CF	A	LDA A AC1AD
2				OPT LSKP	147	0050	06 5E		LDA A #15
3				*****	148	0052	0D 02D0	I	JSH OUTCH
4				* PROTOTYPE GUARD MONITOR PROGRAM	149				*
5				* VERSION 2.0 01/04/76	150				* READ TTY LINE (BUFPTR)
6				* COPYRIGHT 1976 BY AMERICAN MICROSYSTEMS INC.	151				* STORE TTY INPUT IN BUF UNTIL CR IS HIT
7				*****	152				*
8				* DEFINITIONS	153	0055	CE F140	A	LDA #BUF
9					154	0056	FF FF0A	A	SIX BUFPTR
10					155	0058	00		SEC
11					156	005C	74 FFE4	A	LUL ECHO FLAG
12					157				* BEGIN UNTIL LOOP
13					158	005F	0C F107	A	W110 CPA #BUF+71
14					159	0062	26 02		BNE RT20
15					160	0064	28 47		BRA #A301
16					161	0066	50 0000	I	R120 JSH
17					162	0069	47 00		R130 STA A,0,x
18					163	006B	0H		LDA #A
19					164				* WHILE CONDITION 1
20					165	006C	01 00		W190 CMP A #CR
21					166	006E	26 1F		BNE RT10
22					167				* END OF LOOP
23					168				*
24					169				* DECODE 1 CHAN COMMAND
25					170				* CUMPAKE CHAN WITH TABLE OF VALID CHARS FOLLOWED BY
26					171				* ADDRESSSES OF APPROPRIATE ROUTINES.
27					172				*
28					173	0070	0D 0305	I	JSH #X1515
29					174	0073	08		INX
30					175	0074	FF FF0A	A	SIX BUFPTR
31					176	0077	CE 000C	I	LDA #CTABLE
32					177				* BEGIN LOOP
33					178	007A	41 00		DLLOOP CMP A,0,x
34					179	007C	26 04		BNE DL10
35					180				* FOUND CHAN. GET ADDRESS IMMEDIATELY FOLLOWING CHAN.
36					181	007E	EE 01		LDA #A
37					182	0080	0E 00		CMP #A
38					183				* NO CUMPAKE. MOVE TO NEXT CHAN.
39					184	0082	08		DL10
40					185	0083	08		INX
41					186	0084	28 47		BRA #A301
42					187	0085	0C 00AD	I	CPA
43					188	008B	26 F0		BNE DL20P
44					189				* END LOOP.
45					190	008A	20 21		BRA #A301
46					191				* NUT IN TABLE.
47					192				*
48					193				* SUBR IS A MACRO TO CALL RSRSR ROUTINES
49					194				*
50					195				* TABLE: TABLE OF VALID 1 CHARACTER COMMANDS.
51					196				* EACH ENTRY CONSISTS OF 3 BYTES. BYTE 1
52					197				* CONTAINS THE ASCII CHAR. BYTES 2,3 CONTAIN THE
53					198				* ADDRESS OF THE APPROPRIATE ROUTINE.
54					199				*
55					200				* MONITOR RAM
56					201	008C	4C		BYTE #L
57					202	008D	00AD	I	ORAU EQU #A
58					203	008F	00		BYTE #C
59					204	0090	014F	I	ORAU #D
60					205	0092	50		BYTE #P
61					206	0093	030E	I	ORAU #PUNCH
62					207	0095	42		BYTE #B
63					208	0096	0001	H	ORAU BURN
64					209	0098	40		BYTE #M
65					210	0099	0002	M	ORAU MOVE
66					211	009B	50		BYTE #V
67					212	009C	0004	H	ORAU VFY
68					213	009E	40		BYTE #I
69					214	009F	0005	R	ORAU READ
70					215	00A1	53		BYTE #S
71					216	00A2	03E3	I	ORAU SM
72					217	00A4	40		BYTE #O
73					218	00A5	0136	I	ORAU DM
74					219	00A7	52		BYTE #R
75					220	00A8	000E	I	ORAU PNEGS
76					221	00A9	45		BYTE #E
77					222	00AB	0150	I	ORAU EOF
78					223	00AD	1		CTEND EQU *
79					224				*
80					225				* *****
81					226				* ABORT
82					227				*
83					228				* *****
84					229				*
85					230				* USER SWI VECTOR (MAY NOT BE IMPLEMENTED)
86					231				* INDIRECT POINTING TO ACIA FOR RSRSR
87					232				* INTERRUPT REQUEST VECTOR
88					233	0041	CE 0275	I	ORAU EQU #A
89					234				* SOFTWARE INTERRUPT VECTOR
90					235				* UN-MASKABLE INTERRUPT VECTOR
91					236				* *****
92					237				* *****
93					238				* *****
94					239				* *****
95					240				* *****
96					241	00B5	20 8A		BRA #NONENI
97					242				*
98					243				* *****
99					244				* *****
100					245				* *****
101					246				* *****
102					247				* *****
103					248				* *****
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105					250				* *****
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110					255				* *****
111					256				* *****
112					257				* *****
113					258				* *****
114					259				* *****
115					260				* *****
116					261				* *****
117					262				* *****
118					263				* *****
119					264				* *****
120					265				* *****
121					266				* *****
122					267				* *****
123					268				* *****
124					269				* *****
125					270				* *****
126					271				* *****
127					272				* *****
128					273				* *****
129					274				* *****
130					275				* *****
131					276				* *****
132					277				* *****
133					278				* *****
134					279				* *****
135					280				* *****
136					281				* *****
137					282				* *****
138					283				* *****
139					284				* *****
140					285				* *****
141					286				* *****
142					287				* *****
143					288				* *****
144					289				* *****
145					290				* *****


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291 00E4 AF 00 * STS 0,x
292
293 * A STILL CONTAINS S+1 INDEX. TEST IT
294
295 00E6 01 01 CMH A #129
296 00E8 20 04 BNE PREGS NOT 129: BREAK
297 00EA 80 07 BSR PRI 129: SNAPSHOT
298 00EC 20 1E BNA RESTAK AND RETURN TO USER PROGRAM
299
300 *
301 *****
302 * PREGS: PRINT USER REGISTERS
303
304 *****
305
306 00EE 80 03 PRELS EQU * PRI
307 00F0 7E 0047 I BSH JMP MONEND
308 00F3 I PRI EQU *
309 00F3 CE FFE8 A LDX #CREG SUBROUTINE TO PRINT REGS
310 * PRINT 3 1-BYTE REGS X POINTS TO 1ST BYTE OF AREA
311 LDA B #3
312 00F6 C6 03 * SET UP COUNT
313
314 00F8 *
315 00FA 80 03B0 I PH10 SUBM P2HEX PUSH INTO USER STACK
316 00FD 5A JSM PSPACE
317 00FE 2E F8 BGT PRI0
318
319 * PRINT 3 2-BYTE REGS
320 LDA B #3 SET UP COUNT
321
322 0102 80 037C I PH20 JBR P4HEX
323 0105 5A DEC B
324 0106 2E FA BGT PR20
325
326 0108 80 0304 I JSM PCRLF PRINT CRLF
327 0109 39 WTS RETURN
328
329 *****
330 *
331 *****
332 * MESSAGE USER STATUS AND RETURN FROM MONITOR
333
334 *****
335 * MESSAGE USER'S STATUS
336
337 *****
338 *****
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340 *****
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445 0107 40 4E LDA A ADDR+BASE,x MSGTYPE
446 0109 20 4F LWA B ADDR+1-BASE,x
447 010B C3 4D SHL B ADDR+1-BASE,x
448 010D 42 4C BNC * ADDR+BASE,x
449 010F 24 06 BEC GETREG ADDR+BASE,x
450 0111 CE 0265 I MNGER LWA #MNGER ADDR+BASE,x
451 0113 7E 0000 I JMP MSG+ABORT
452
453 0197 FE FF0E A LETHW LUX ADDR INC ADDR
454 0199 06 LWA B ADDR
455 019B FF FF0E A INX STA
456 019E 39 WTS
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458 *****
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Advanced Microcomputer Products Presents

Prototype Design Equipment

CONTRIBUTOR'S COMPARISON

AT SOCKETS AND BUS STRIPS

... (Detailed list of products and prices) ...

PHOTO-BOARD 100 KIT

... (Detailed description of the kit) ...

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- EVK 99** consists of the following only:
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(1) 6800 ACIA (Asynchronous Communication Interface Adapter)
(1) 6800 PIA (Peripheral Interface Adapter)
(1) 6800 ROM Subroutine Program Library (16831 16K ROM)
(1) 6801 I/O RAM
(1) Owner's Manual & Instructions
- UNIVERSAL KLUGE BOARD \$98.00**
Completely compatible to the EVK system. This board allows the user to add any additional parts he desires. It has 540 holes, holds 94 16 Pin IC's or others on a 4, 6, 8, 10 pin connector. 2 50 pin 1 20 pin 1 25 pin 8022 connector.
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16K x 8-Bit 16 organization. User 17022 and adapt to 16m memory.
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LM106H	80	LM320K 1/5	145	LM392N 1/10	1.79	LM4145CN	35	LM4545CN
LM106H	45	LM320K 1/10	145	LM392N 1/20	1.79	LM4145CN	35	SG3524
LM106H	125	LM320K 1/20	145	LM392N 1/50	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/50	145	LM392N 1/100	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/200	145	LM392N 1/200	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/500	145	LM392N 1/500	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/1000	145	LM392N 1/1000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/2000	145	LM392N 1/2000	1.79	LM4145CN	35	LM4545CN
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LM106H	120	LM320K 1/20000000000000000000000	145	LM392N 1/20000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/50000000000000000000000	145	LM392N 1/50000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/100000000000000000000000	145	LM392N 1/100000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/200000000000000000000000	145	LM392N 1/200000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/500000000000000000000000	145	LM392N 1/500000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/1000000000000000000000000	145	LM392N 1/1000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/2000000000000000000000000	145	LM392N 1/2000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/5000000000000000000000000	145	LM392N 1/5000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/10000000000000000000000000	145	LM392N 1/10000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/20000000000000000000000000	145	LM392N 1/20000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/50000000000000000000000000	145	LM392N 1/50000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/100000000000000000000000000	145	LM392N 1/100000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/200000000000000000000000000	145	LM392N 1/200000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/500000000000000000000000000	145	LM392N 1/500000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/1000000000000000000000000000	145	LM392N 1/1000000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/2000000000000000000000000000	145	LM392N 1/2000000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/5000000000000000000000000000	145	LM392N 1/5000000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/10000000000000000000000000000	145	LM392N 1/10000000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/20000000000000000000000000000	145	LM392N 1/20000000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/50000000000000000000000000000	145	LM392N 1/50000000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/100000000000000000000000000000	145	LM392N 1/100000000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/200000000000000000000000000000	145	LM392N 1/200000000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/500000000000000000000000000000	145	LM392N 1/500000000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/1000000000000000000000000000000	145	LM392N 1/1000000000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/2000000000000000000000000000000	145	LM392N 1/2000000000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/5000000000000000000000000000000	145	LM392N 1/5000000000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/10000000000000000000000000000000	145	LM392N 1/10000000000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/20000000000000000000000000000000	145	LM392N 1/20000000000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/50000000000000000000000000000000	145	LM392N 1/50000000000000000000000000000000	1.79	LM4145CN	35	LM4545CN
LM106H	120	LM320K 1/100000000000						


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028E 3030
0290 3030
0292 4045
597 0294 04
598 0295 000A MCR LFS BYTE 4 CR,LF,0,0,0,0,'S','I',4
0297 0000
0299 0000
029B 5331
029D 04
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597 0294 04
598 0295 000A MCR LFS BYTE 4 CR,LF,0,0,0,0,'S','I',4
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MICROCOMPUTER DEVELOPMENT SOFTWARE

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227 0540 A0 00 L L0A4 0,X
228 0542 C8 F8L0 A L0A #PIA
229 0545 A7 00 STAA PR2M+2,X
230 0547 A8 05 L0A4 PR2M+1,X
231 0549 04 F7 AN0A #B*1110111 SET N/A TO N
232 054B A7 05 STAA PR2M+1,X
233 054D A0 07 L0A4 PR2M+3,X
234 054F 04 F8 AN0A #B*1110111 TURN IT AROUND
235 0551 A7 07 STAA PR2M+3,X (TO OUTPUTS)
236 0553 0F 06 CLR PR2M+2,X
237 0555 03 06 COM PR2M+2,X
238 0557 37 F3MD
239 0558 C0 14 L0A4 #20
240 055A 00 3F BSR #SEC CLEAR TIME#
241 055C 00 36 BSR #SEC WAIT 1 MS BETWEEN PULSES
242 055E A8 01 L0A4 V50,X
243 0560 04 F7 AN0A #B*1110111 SET HIGH VOLTAGE
244 0562 A7 01 STAA V50,X
245 0564 00 35 BSR #SEC 1 MS PULSE DURATION
246 0566 00 33 BSR #SEC
247 0568 00 31 BSR #SEC
248 056A 01 00 UAAA #R*0011000 TURN OFF HIGH VOLTAGE
249 056C A7 01 STAA V50,X
250 056E 54 UEL0
251 056F 26 0E CLC #IF 20 TIMES,
252 0571 0F 00 BSR PR2M+2,X CONVERT OUTPUTS TO INPUTS
253 0573 A5 05 L0A4 PR2M+1,X TURN OFF WHITE
254 0575 04 30 UAAA #R*0011000
255 0577 A7 05 STAA PR2M+1,X
256 0579 00 10 IF DELAY
257 0579 C0 0A L0A4 #DELAY
258 057B 00 11 BSR #SEC DELAY (B) MS
259 057D 54 DEC0
260 057E 26 F8 GNL #IF
261 0580 00 33 PUL0
262 0581 00 00 00 01 JSV VFTI CHECK IT:
263 0584 24 0F BVS :J BAD BIT SHOWED UP
264 0586 2F A0 BVL :I GOOD
265 0588 00 21 IF #0 NO TYPE A NAK
266 0588 80 15 L0A4 #21 0
267 058A 00 * IEND
268 058A 3F * CALL PRINTA
269 058B 11 * SWI
270 058B 00 * BYTE PRINTA
271 058C CE F8C0 A GNL #PIA
272 058F 51 UEL0 AND TRY AGAIN
273 0590 26 AB BSR TL
274 0592 00 04BF I J EQV VERR
275 0595 7E 0005 R JBAD JSR #JMP
276 0598 7E 0009 R NUQ000 JMP ABORT
277 0598 60 05 #SEC TSI PROM+1,X
278 059D 24 FC BPL #SEC
279 059F A7 04 CWP A PROM+X
280 05A1 39 #IS CLEAR IF (WITH A DATA READ)
281 *
282 * MEMORY MOVE
283 *
284 05A2 00 0101 R I IF MOVER
285 05A5 00 0002 R MOVE JSR GETRNG GET SOURCE ADDRESS RANGE
286 05A8 27 1B BVS JSR VTTADR GET DESTINATION STARTING ADDRESS
287 05AA 28 18 L0A4 JBAD ENQW IF NONE
288 05AB 05A8 FE 000D R #IF XAD ADOL GET BYTE
289 05AD A0 80 L0A4 0,X
290 05AF FE 000C R LDI ADDR
291 05B2 80 000D R JSR SETEM STORE IT WITH VERIFY
292 05B5 00 INX
293 05B6 FF 000C R STX AUK INCREMENT POINTERS
294 05B9 00 04F1 I JSR AUK
295 05BC 20 EC BRA #M COMPARE TO END
296 05C0 00 00 ELSE #IF MORE
297 05C2 00 00 EAU HMM
298 05C4 00 00 LEND
299 *
300 * END IF MODULE
301 *
302 END

```

SYMBOL TABLE:

ABORT	0009 R	ADLM	000E R	ADDL	000D R	ADRS	04B2 I
ADR	000C R	BURN	0510 I	CUUNT	000F R	DELAY	000A R
EXIT	04F0 I	GETRNG	0001 R	INCRAB	04E4 I	INX	04F1 I
JBAD	0509 R	UVER	0511 I	NUQENT	000D R	MONTR	000A R
MOVE	05A2 I	MOVER	0001 A	#SEC	0505 I	NUQ000	0598 I
PR2ADR	0002 R	PAHEX	0010 A	PR2IN	0030 I	PR2ADR	0005 R
PCFLP	0006 R	PIA	F8C0 A	IN11	0011 I	PRINTA	0011 A
PR2M	0004 A	PR2MD	000D R	PR2P	0043 I	PSPACE	0007 R
PR2STS	0003 R	RAM	FC00 A	V50	0400 I	WEL0	0400 I
PR2LDR	0014 R	ST1	FE00 R	Y50	0001 A	WEH	0400 I
VFT	04C4 I	VFTI	0000 I				

CHECKSUM = 9580

LENGTH OF ISEC1 = 0 (U000)
 LENGTH OF ISEC2 = 424 (V1AB)

NO ERRORS, NO ABORTS, THIS ASSEMBLY

VECTORED FROM PAGE 101			
AGE, DEC. 1976, VOL.1, #13.			
8080	AMS80	AMSAT 8080 STANDARD DEBUG MONITOR BY RICHARD C ALLEN & JOE KASSER - BYTE # 13, SEPT. 1976, VOL.2, #1. SUBMITTED BY JOE KASSER.	31-PTSL < 2 10.00+0.60+2.00 31-PTOD < 3.00+0.18+1.75 31-PACK ↑
6800	BAFCMP	BASIC ALGORITHMS FOR COMMON MATH FUNCTIONS BY MICHAEL P. BURTON - INTERFACE AGE, JAN. 1977, VOL.2, #1.	32-PTBL < 1 3.00+0.24+1.00 32-TEXT < 1.00+0.06+1.00 32-PACK ↑
8080	ECMSO	MICROCOMPUTER STOCK OPTIONS BY EDWARD CHRISTIANSON - INTERFACE AGE, FEB. 1977, VOL.2, #3.	33-PTBL < 0 6.00+0.36+2.00 33-HCBLF 2.00+0.12+1.25 33-HCBLF< INC. WITH PTBL 33-TEXT < 33-PACK ↑
8080	BM RNG	RANDOM NUMBER GENERATOR BY BOB MARTIN - INTERFACE AGE, FEB. 1977, VOL.2, #3.	34-PTAL < 0 6.00+0.36+2.00 34-PTSL < 5.00+0.30+1.75 34-TEXT < 1.00+0.06+1.00 34-HCALF 1.00+0.06+1.00 34-HCALF< INC. WITH PTAL
8080	RNDFGCST	RND FUNCTION GENERATOR CHI-SQUARE TEST PROGRAM BY BOB MARTIN - INTERFACE AGE, FEB. 1977, VOL.2, #3.	35-PTBL < 3.00+0.18+1.00 35-HCBLF< INC. WITH PTBL 35-PACK ↑
8080	TTMOCSR	8080 MEMORY OBJECT CODE SEARCH ROUTINE BY T. E. TRAVIS - INTERFACE AGE, FEB. 1977, VOL.2, #3.	36-PTAL < 0 3.00+0.18+1.00 36-PTSL < 3.00+0.18+1.00 36-TEXT < 1.00+0.06+1.00 36-HCALF< INC. WITH TEXT 36-HCALF 1.00+0.06+1.00 36-PACK ↑
8080	TDOMP	8080 OCTAL MONITOR PROGRAM BY THOMAS E. DOYLE - INTERFACE AGE, FEB. 1977, VOL.2, #3.	37-PTAL < 0 8.00+0.48+2.00 37-PTSL < 6.00+0.36+1.75 37-TEXT < 2.00+0.12+1.00 37-HCALF< 2.00+0.12+1.00

VECTORED FROM PAGE 101			
AGE, DEC. 1976, VOL.1, #13.			
8080	AMS80	AMSAT 8080 STANDARD DEBUG MONITOR BY RICHARD C ALLEN & JOE KASSER - BYTE # 13, SEPT. 1976, VOL.2, #1. SUBMITTED BY JOE KASSER.	31-PTSL < 2 10.00+0.60+2.00 31-PTOD < 3.00+0.18+1.75 31-PACK +
6800	BAFCMP	BASIC ALGORITHMS FOR COMMON MATH FUNCTIONS BY MICHAEL P. BURTON - INTERFACE AGE, JAN. 1977, VOL.2, #1.	32-PTBL < 1 3.00+0.24+1.00 32-TEXT < 1.00+0.06+1.00 32-PACK +
8080	ECMSO	MICROCOMPUTER STOCK OPTIONS BY EDWARD CHRISTIANSON - INTERFACE AGE, FEB. 1977, VOL.2, #3.	33-PTBL < 0 6.00+0.36+2.00 33-HCBLF 2.00+0.12+1.25 33-HCBLF< INC. WITH PTBL 33-TEXT < 33-PACK +
8080	BM RNG	RANDOM NUMBER GENERATOR BY BOB MARTIN - INTERFACE AGE, FEB. 1977, VOL.2, #3.	34-PTAL < 0 6.00+0.36+2.00 34-PTSL < 5.00+0.30+1.75 34-TEXT < 1.00+0.06+1.00 34-HCALF 1.00+0.06+1.00 34-HCALF< INC. WITH PTAL
8080	RNDFGCST	RND FUNCTION GENERATOR CHI-SQUARE TEST PROGRAM BY BOB MARTIN - INTERFACE AGE, FEB. 1977, VOL.2, #3.	35-PTBL < 3.00+0.18+1.00 35-HCBLF< INC. WITH PTBL 35-PACK +
8080	TTMOCSR	8080 MEMORY OBJECT CODE SEARCH ROUTINE BY T. E. TRAVIS - INTERFACE AGE, FEB. 1977, VOL.2, #3.	36-PTAL < 0 3.00+0.18+1.00 36-PTSL < 3.00+0.18+1.00 36-TEXT < 1.00+0.06+1.00 36-HCALF< INC. WITH TEXT 36-HCALF 1.00+0.06+1.00 36-PACK +
8080	TDOMP	8080 OCTAL MONITOR PROGRAM BY THOMAS E. DOYLE - INTERFACE AGE, FEB. 1977, VOL.2, #3.	37-PTAL < 0 8.00+0.48+2.00 37-PTSL < 6.00+0.36+1.75 37-TEXT < 2.00+0.12+1.00 37-HCALF< 2.00+0.12+1.00

AN 8080 MEMORY OBJECT CODE SEARCH ROUTINE

By T. E. Travis

NEED FOR OBJECT CODE SEARCH ROUTINE

When attempting to modify software, it is often necessary to find and change every occurrence of a particular instruction sequence or every reference to some specified memory location. For example, if one wished to modify a teletype-oriented BASIC to use one of the available memory mapped video boards such as the Polymorphics VTI-1, it would be necessary to find all IN and OUT instructions directed toward the teletype port and change them to calls to input and output drivers for the video board. Since, in the case of vendor supplied software, a source listing of the program to be modified is often not available, a program to search through memory looking for and identifying all such calls is necessary.

SEARCH PROCESS

The program presented here requires no peripherals and will search memory starting at any desired location looking for a byte pattern of any arbitrary length. Every time the pattern is found, the program

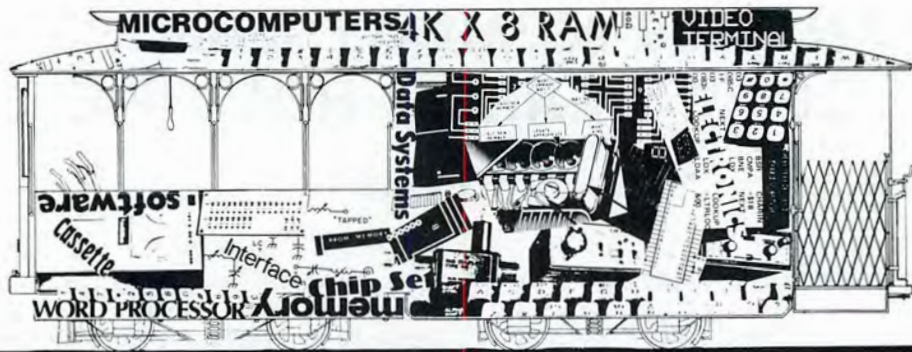
stops with the address of the first byte *following* the pattern in memory locations 26 and 27 (hex). Once those locations have been examined and noted, the program can be restarted and it will continue its search.

APPLICATION

As listed, the program begins at location zero, but it can be moved to any place in memory by changing all of the three byte instructions to point to their new targets. To use the program, load the starting address into memory locations 26 and 27, the length of the pattern into 28, and the pattern to be sought into 29 to 29 + n where n is the value stored in 28. The program is then initiated at location zero and will stop when it encounters the desired pattern. This will always happen because the program will eventually wrap around memory and compare the pattern with itself.

SEE MICROCOMPUTER SOFTWARE DEPOSITORY PROGRAM INDEX FOR COPIES OF THIS PROGRAM.

8080 MACRO ASSEMBLER, VFR 2.3 ERRORS = 0 PAGE 1									
<pre> PROGRAM NAME: SERCH (8080 MEMORY SEARCH ROUTINE) PROGRAMMER: T. E. TRAVIS STORAGE REQUIREMENTS: 41 BYTES PLUS PATTERN I/O REQUIREMENTS: NONE REQUIRED SUPPORTING SOFTWARE: NONE </pre>									
0000		SERCH	FOU	\$					
0000	2A2600	CONT	LHLD	\$	ADDR				:LOAD STARTING ADDRESS
0003	112900		FOU	\$:LOAD PATTERN ADDRESS
0006	3A7800		LXI	D	PATRN				:LOAD PATTERN LENGTH
0009	47		MVI	B	A				:MOVE LENGTH TO B
COMPARE PATTERN WITH MEMORY									
000A		COMP	FOU	\$:LOAD PATTERN BYTE
000A	1A		LDAX	D					:COMPARE WITH MEMORY
000B	BF		CMP	H					:BRANCH IF NOT EQUAL
000C	C21800		JNZ	NOTFO					:INCREMENT MEMORY POINTER
000F	73		INX	H					:INCREMENT LENGTH COUNTER
0010	05		DLP	D					:BRANCH IF DONE
0011	C42700		JT	EQUAL					:INCREMENT PATTERN POINTER
0014	13		INX	D					:CONTINUE TESTING
0015	C30A00		JMP	COMP					
PATTERN DID NOT COMPARE, ADVANCE MEMORY STARTING ADDRESS									
0018		NOTEQ	FOU	\$:LOAD STARTING ADDRESS
0018	2A2600		LHLD	\$	ADDR				:INCREMENT
001A	23		INX	H					:SAVE
001C	222600		SHLD	ADDR					:START TEST AGAIN
001F	C30300		JMP	CONT					
PATTERN DID COMPARE									
0022		EQUAL	FOU	\$	ADDR				:SAVE HALT ADDRESS
0022	222600		SHLD	ADDR					:HALT
0025	76		HLT						
0027		ADDR:	DS						:MEMORY START ADDRESS
0001		LNTH:	DS						:PATTERN LENGTH
0001		PATRN:	DS						:TEST PATTERN
WHEN PATTERN FOUND, PROGRAM STOPS WITH ADDR POINTING TO FIRST BYTE FOLLOWING PATTERN									
END									
NO PROGRAM ERRORS									
8080 MACRO ASSEMBLER, VFR 2.3 ERRORS = 0 PAGE 2									
SYMBOL TABLE									
* 01									
A	0007	ADDR	0026	\$	0000	C	0001		
COMP	000A	CONT	0003	D	0002	E	0003		
EQUAL	0022	H	0004	L	0005	LNTH	0008		
M	0006	NOTFO	0018	PATRN	0027	PSW	0006		
SERCH	0000	SP	0006						



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Letters to the Editor

Dear Editor:

I am a professional programmer and have been vaguely aware of the existence of the personal computer for about a year. Last week, while shopping, I passed by a computer store and stopped in to satisfy my curiosity. After looking at the system and reading some magazines, I left in a state of amazement and joy after discovering all of the hardware and software available to the home computerist. I'm very happy about finding a hobby that I can really "get into." For my first project, I would like to convert a B & W TV set into a video monitor. If any of the INTERFACE readers have any suggestions as to how to accomplish this task, I would be grateful to hear from them.

Brian O'Connell

Dear Editor:

I am writing this letter to inform the readers that the MITS-BASIC Software package will not run with the Z80 processor.

The problem has to do with the use of the parity flag. MITS seems to use it extensively.

I was wondering if any of your readers had some sort of a solution for this problem.

Joe T. Huffman

No sooner said than done — See the article A Z80 MITS 12K Extended BASIC Patches, by Martin D. Gray in this issue of INTERFACE AGE. This article provides required software patches to the MITS Extended BASIC for execution by the Z80 CPU.

Software Editor

Dear Editor:

... I am an inmate in the Washington State Penitentiary... Several of us here are trying to utilize our time by studying computers.

NAME WITHHELD

Dear Editor:

Thanks for publishing Dr. Wang's Palo Alto Tiny Basic in a more readable form than that which appeared in Dr. Dobb's Journal.

There is a glitch in the change sign routine which gives the "HOW" error message whenever a zero value or expression is preceded by a minus sign. For example: LET A = 0; Let B = -A will not work.

To fix this change the CHGSGH routine at 0486 by adding three instructions:

CHGSGN:

```

                                MOV  A,H
added instructions { ORA  L
                    RZ      ;zero value
                    MOV  A,H
                    PUSH PSW

```

Arthur I. Larky PH. D

Dear Editor:

I have just started to read INTERFACE magazine and find it very difficult to put down. I really enjoy reading the articles that discuss the new versions of Star Trek that are becoming available and all the other articles that discuss various programs (Basic-diet-plan) and others. I am really amazed how you can just list the proper bits of information and just start plugging them right into the old computer banks. I am also glad that you put all your games and other lists in 8K Basic. I am going to be purchasing a IMSAI 8080 or an ALTAIR 8800b in the near future and through your magazine alone I will be able to start developing a library immediately.

There is a new topic I would really like to see discussed and that is the possibility and availability of voice recognition boards and apparatus for microprocessor like the IMSAI 8080 and the ALTAIR 8800b. I would really be fascinated and I would feel that investment into the microprocessors would be a good idea cause I could eventually expand it into a unit using voice recognition equipment as a peripheral.

Also is there a good book around that will teach me how to understand and use 4K BASIC all the way through extended BASIC (12K)? I would like a book that presents this information clearly and simply. I am looking forward to hearing from you very soon. I really hope to see an article about voice recognition and all its hardware come up soon. I just sent my subscription in to your magazine today so I won't miss any of the other exciting things you already put in your magazine. Thank you for your time.

Douglas Call

Dear Editor:

In that I am a beginner in computers and working with a small budget, I would like to see more how-to articles in your magazine. I cannot afford a language system right now, and since I'm starting from scratch with only a communications background, I am writing very simple iterations in machine language. I'm building an octal terminal for a little more speed in my programming. Your magazine seems to have a particular wealth of advertizements and a dearth of instruction and theory. Articles of some length on such things as instruction sets, and basic routines would be very welcome.

I am a technician in the Navy, and somewhat handicapped by a lack of literature overseas and the great cost of technical publications. I know that there are quite a few of us in the same situation. It is very difficult to learn microcomputers this way. I will be very happy to write you some articles when I learn something!

John Fitzpatrick

Dear Editor:

An article I would like to see in INTERFACE AGE would be about the use of hobbyist type equipment to solve some of the basic 'real world' problems of operating a robot in a house or shop type environment. Problems such as fail safe design, telemetry, navigation, and hazard avoidance.

Paul F. Grayson

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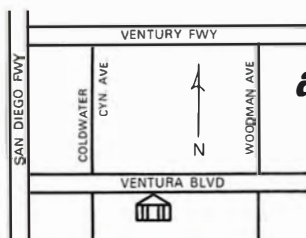
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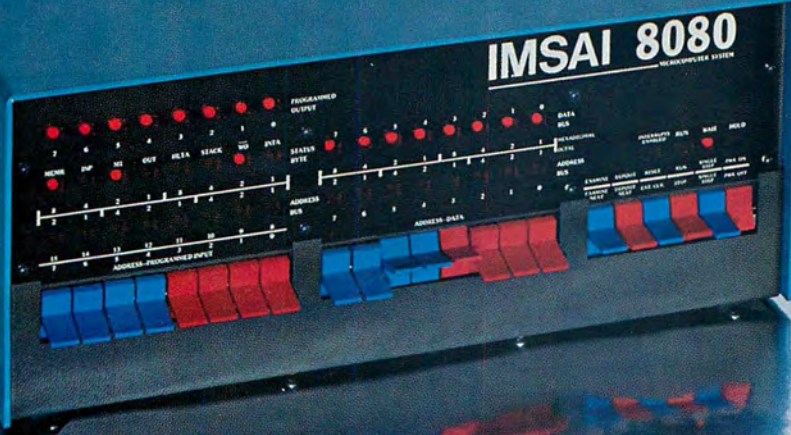
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